ESTIMATION AND OPTIMIZATION OF LAYOUT PARASITICS FOR SILICON-BASED MILLIMETER-WAVE INTEGRATED CIRCUITS

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ESTIMATION AND OPTIMIZATION OF LAYOUT PARASITICS FOR SILICON-BASED MILLIMETER-WAVE INTEGRATED CIRCUITS

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My Mother:

For her constant love, support, and sacrifices.

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Summary

Millimeter-wave has been a medium for automotive, sensor, and defense applications for a long time. But, a fully integrated silicon-based transceiver at 60 GHz or higher frequencies has become the driving force for recent research activities in integrated millimeter-wave (MMW) circuit designs. License-free frequency bands are essential for any viable commercial applications. The worldwide license-free 59-64 GHz band is the most suitable one to support multi-gigabit transmission over 1 m - 10 m distance. However, no integrated compact high-performance millimeter-wave system can be designed without accurate estimation and optimization of layout parasitics.

In this dissertation, the estimation, modeling and optimization of parasitic effects as well as the verification of extraction methodologies for RF/MMW applications are investigated. Different circuit design- and layout-examples are considered with stress on the inclusion and optimization of wire/interconnect parasitics. A novel methodology is proposed to reduce the number of design-passes and to include layout parasitics in the design optimization procedure. An automated verification procedure for existing parasitic extraction tools is developed. Neural-network-based models are used to demonstrate the effectiveness of artificial intelligence techniques for characterizing parasitic components. The parasitic sensitivities for selected millimeter-wave circuits are demonstrated, and a parasitic benchmarking procedure is developed using MMW oscillators. Measurement results of several circuits that are implemented in state-of-the-art CMOS and SiGe-BiCMOS processes are used to demonstrate the role of parasitics and the systematic design methodology including parasitics.

Chapter 1

Introduction

1.1 Motivation

The rapid advancements in semiconductor technologies have enabled the design of high-performance integrated systems at millimeter-wave frequencies to meet the increasing demands of the present wireless-communication industry. Millimeter-wave media have been used for automotive, sensor, and military applications for a long time. Although military and defense applications use either 77 GHz or higher carrier frequencies, the license-free frequency bands are essential for any viable commercial applications. The bandwidth of the frequency band should also be large enough to be able to support a multi-gigabit transmission over a 1 m - 10 m distance. Hence, tremendous potential exists for using the 57-64 GHz unlicensed frequency band (59-64 GHz worldwide) for high-speed data transfer between storage devices, point-to-point video, HDTV, and wireless personal-area-networking (WPAN) applications [1.1]. This bandwidth is wide enough to achieve multi-gigabit wireless transmissions using simple modulation schemes, e.g., amplitude-shift keying (ASK) and binary phase-shift keying (BPSK). More complex schemes, e.g., quadrature phase-shift keying (QPSK) and orthogonal frequency-division multiplexing (OFDM), can result in a data rate higher than 10 Gbps. Historically, 60 GHz electronic components were only feasible in expensive

and bulky compound semiconductors. To achieve a widespread adoption of 60 GHz technologies, it is necessary to implement these circuits in low-cost technologies such as complementary metal-oxide-semiconductor (CMOS) or silicon-germanium (SiGe) hetero-junction bipolar transistors (HBTs).

However, with the increase of operating frequencies in integrated circuits (ICs), the layout parasitics need immediate attention. The interconnect parasitics degrade circuit performance, and their estimation and optimization have also become an important part of the design and layout optimization for millimeter-wave (MMW) applications. The recent interest [1.1, 1.2] in integrated systems for ultra-wide-band (UWB) and 60-GHz-WPAN applications demands good performance from both active and passive components at these frequencies.

Silicon (Si)-based technologies have a winning edge over commercial gallium arsenide (GaAs)-based technologies in terms of lower cost and integration of the RF front-end with the baseband circuitry. The constant shrinking of the minimum feature size in today's sub-micron Si-based technologies has the potential to meet the demands of MMW systems. However, the performance limitations of active devices at millimeter-wave frequencies in silicon-based processes necessitate an accurate characterization of the transmission lines and interconnects that are incorporated in the layouts of integrated circuits.

Electro-magnetic (EM) simulation techniques that have been developed over the past decade for high-frequency structures have enabled the use of the computer-aided design (CAD) for hybrid and monolithic integrated RF/microwave circuits. The accurate

estimation of the parasitic effects can result in the first-pass success of the embedded micro-strip/co-planner-waveguide (CPW)-line-based integrated MMW circuits.

Parasitic modeling in active devices and interconnects is a critical step in the design flow of multi-layer ICs [1.3,1.4]. There are several approaches to extract the parasitic resistance-inductance-capacitance (RLC) networks and to include them in the circuit design/simulation. For the available electromagnetic (EM) and non-EM solvers, the trade-off parameters are the accuracy and the extraction time. EM tools, e.g., Momentum, HFSS, and IE3D, are more accurate, but the extraction times for these tools are lengthy, and it is difficult to include the extracted networks in a circuit-level simulation environment. However, the analytical model-based non-EM solvers, e.g., Calibre XRC, Assura RCX, and Star RCXT, are popular for their fast execution time and easy application in circuit-level simulations. Even today, with all the advancements in tools and technologies, there are only a few analytical-model-based parasitic-inductance extraction tools, and they are much slower than their counterparts. The unwanted inductances play an important role in the design accuracy for frequencies higher than 10 GHz.

The layout optimization for parasitics is an important step in the design of MMW ICs. To satisfy the design rules in a multi-layer process, most of the parasitics are unavoidable, and minimization of all the parasitic components is not always possible nor it is essential. In an integrated-system approach, the large number of transmission lines and pad connections makes the layout optimization difficult. The transmission lines are usually realized in the top metal layers and are used for matching or tuning the circuits. Active devices require 3D interconnects as they are connected to the lower metal levels.

The nodes and signal paths need to be determined at the points where the parasitic effects are most pronounced.

Thus, the design of millimeter-wave integrated circuits cannot be optimized until the effects of the wire parasitics are taken care of. Since not all parasitic effects denigrate the circuit performance, it is a misconception to minimize all parasitics to optimize a design. However, the identification of significant interconnect components and the optimization of the dimensions according to circuit performances are essential steps in the design flow.

1.2 Aim and approach

There are two different topologies to deal with parasitics. The topologies are represented in Figure 1.1. The standard topology is to extract some parasitics and later, from the measurement results, to re-tune the circuit to meet the specifications in consecutive fabrication runs. The other topology (the one proposed in this work) deals with the extraction and optimization of parasitics and accordingly, redesigning the circuits/systems to reduce parasitic sensitivity. The proposed methodology is shown in Figure 1.1(b).

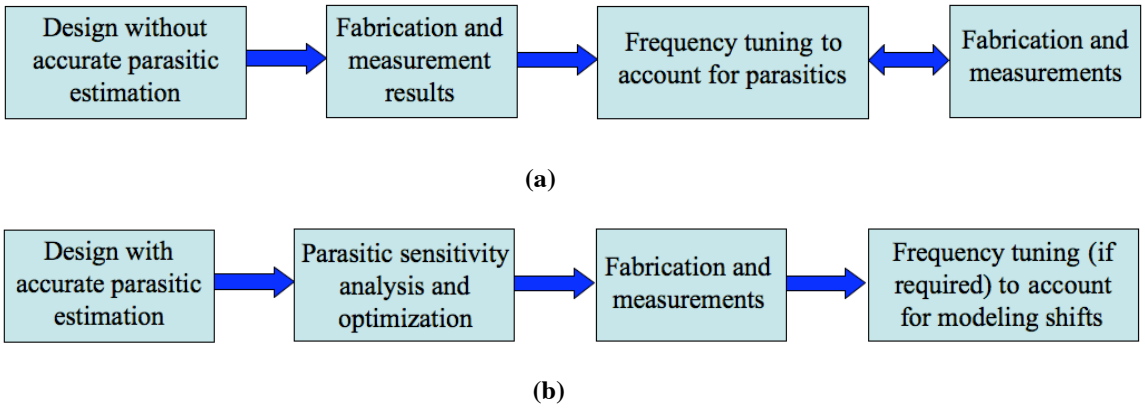


Figure 1.1. The topologies for MMW circuit design including parasitics.

The first topology drives the designer to tune the circuit at higher frequencies and to expect a certain percentage shift. There is always an uncertainty because the parasitic sensitivity of circuits varies a lot with different circuit topologies. The proposed topology suggests an initial layout with estimated parasitics, followed by recursive centering of the design from the sensitivity analysis of parasitics. Design optimization including RLC networks that represent interconnect parasitics can significantly reduce the number of design passes for narrow-band circuits and systems.

Neural-network-based methodologies have already been demonstrated to model the passives in organic polymer (e.g., LCP) and ceramic (e.g., LTCC) processes [1.5, 1.6]. In this work, neural-network-based approach is applied to estimate the wire/interconnect parasitics for RF integrated circuits in state-of-the-art Si-based technologies. In addition, the accuracy of tools, based on the non-EM solving methodology, demands a verification routine that has to be fast, automated, and systematic. A novel and fast verification approach is presented for commercially available parasitic-extraction (PEX) tools.

Silicon-germanium (SiGe) hetero-junction bipolar transistors (HBTs) and 90 nm CMOS devices are primarily chosen for device and circuit analyses. Bandgap-engineered SiGe HBTs exhibit better RF and millimeter-wave performances than bipolar junction transistors (BJTs) of the same size in terms of trans-conductance, noise performance, and small-signal gain. For analyzing the small-signal effects of parasitics, a Gummelpoon-based broadband model [1.7] is developed and used to evaluate interconnect effects. NMOS devices are also tested for the intrinsic parasitics that limit their operation at MMW frequencies. In this work, different circuit examples in these processes are

considered to predict and reduce the shifts from layout parasitics with accurate estimation and optimization.

With the increasingly stringent specifications of wireless transceivers and the ever-increasing carrier frequencies of emerging wireless systems, reliability and production yield have become extremely imperative issues that directly affect the cost and performance of every wireless device [1.8]. As the frequency of operation increases, these issues are aggravated by the increased criticality of the incompletely modeled layout parasitics. This aggravation creates an urgent need for systematic design- and yield-optimization [1.9] procedures, including layout parasitics for the MMW front-ends to improve the production yield and consequently to reduce the time-to-market of future wireless devices.

Hence, for a reliable design, parasitics are sometimes the key components to stabilize the circuits and to reduce the inconsistency caused by process variations. Parasitic inductances and capacitances do not always add to the same effects. They oppose each other, and a precise layout optimization can neutralize or minimize their effects.

1.3 Organization of the thesis

In this work, the issues regarding the estimation and optimization of the layout parasitics have been deciphered for MMW applications. The parasitics are estimated using a neural-network-based model, and an automated extraction procedure for the PEX tools is presented. To optimize the layout parasitics, the interconnect effects in MMW designs are demonstrated for active devices and circuits in Si-based processes. The oscillator serves as a potential test vehicle for this purpose since the oscillation frequency

is extremely sensitive to the layout parasitics and design parameters. Furthermore, to enhance the optimization procedure, the design has to be centered properly with all the significant parasitics taken into account. Hence, it is essential to identify the most sensitive design components. In addition to this sensitivity analysis, a layout and design optimization procedure is proposed based on the design components along with their associated layout parasitics.

The first step in studying the effects of parasitics on the devices, circuits, and systems, is to standardize the parasitic-extraction tools. In the second chapter, the state-of-the-art parasitic-extraction procedure is described. Also the available algorithms for interconnect RLC extractions are studied. The importance of accurate parasitic extraction is explained with examples. The design issues related to basic blocks of MMW systems are presented.

In the third chapter, a verification methodology has been developed using commercially available PEX tools, and the approach is proposed for the developed neural network-based models. A set of multi-layer passive structures is used to verify the tools. The automated layout-generation technique is illustrated using ring oscillators as examples of functional circuits. The initial comparisons are made between commercially available PEX tools, and the final verification of these tools using measurement results is completed using test structures in 90 nm CMOS process. Cross-coupled VCOs are designed, and different versions are fabricated to verify the parasitic-extraction methodology and the transmission-line models. A parasitic-benchmarking procedure is developed to accurately predict the center frequencies and tuning ranges for millimeter-wave VCOs with frequencies varying from 30 to 60 GHz. Neural models are developed

for parasitic elements for interconnect RLC networks and used as an alternative to available PEX tools.

In the fourth chapter, the role of interconnects and the substrate effects on active devices are studied in detail. This study is extended to the parasitic sensitivities of circuit blocks for 60 GHz systems. Circuit layouts are differentiated into two types according to parasitic shifts. The effects of parasitics on the sensitive transceiver blocks are discussed. The design, layout, and parasitic effects on VCOs with different topologies are illustrated in CMOS and HBT technologies. The effects of parasitics are studied for other transceiver blocks like frequency dividers and power amplifiers.

The design optimization is an extremely critical part of millimeter-wave circuit designs. In the fifth chapter, a neuro-genetic algorithm [1.10] is introduced to optimize millimeter-wave circuits. With appropriate sensitivity analyses and layout estimations, the number of variants is reduced. The prediction/characterization of the circuits with these variables is the key component of a layout and design optimization approach for MMW ICs. Layout optimization guidelines are developed for integrated circuits in millimeter-wave frequencies. Later, co-design and co-optimization issues are described for integrated blocks. An integrated up/down converter in SiGe BICMOS process and a VCO-PLL block in a 90 nm CMOS process are implemented to demonstrate the parasitic effects. Finally, parasitic sensitivity of performance parameters is demonstrated for an FSK system at 60 GHz.

The unique research contributions are summarized in the sixth chapter. Later, the future research directions have been presented describing the scope of different methodologies that are developed in this dissertation.

Chapter 2

State of the Art: Parasitic Extraction and Their Role in MMW Circuits

2.1 Overall extraction procedure and state of the art

Electro-magnetic (EM) simulation techniques for high-frequency structures, developed over the past decade have helped to bring the computer-aided design (CAD) for hybrid and monolithic integrated RF/Microwave circuits. The embedded micro strip-line- or coplanar-waveguide (CPW)-line-based integrated MMW circuit design would have been brought to first-pass success level, once, all the parasitic effects can be estimated accurately. Modeling of parasitics in active devices and interconnects is the most critical step in the design flow of multi-layer ICs [1.3, 1.4]. The increased significance of the wire parasitics is mainly because of the following reasons:

- The use of multiple layers for wiring: With the use of transmission lines in the top metal, the layout parasitics are not limited to only two/three metal layers. The via-stacks add complexity to the wiring effects. In addition, higher levels of integration are increasing the chip-area and the interconnect delays.
- The increasing trend of operating frequency with the scaling of technologies, thus allowing a much better active device performances, but at the expense of higher parasitic sensitivity.
- The reliability of the designs, and the need to meet the specifications with minimum number of passes (less time-to-market).

Another trend in millimeter-wave circuits is the increasing need for optimization using design automation. Stringent design specifications demand an optimization procedure using advanced computer algorithms (e.g. genetic) that require iterative circuit evaluation. The design optimization approach is defined by a series of steps, e.g., problem-identification; concept-generation to meet the specifications; analysis; evaluation; initial and optimal designs. In integrated circuits with given specifications, the concepts/topologies are generally evaluated from the theoretical and practical limits, imposed by active devices and the layout parasitics.

In the following sections, the background for the estimation of the layout parasitics and its role in the design flow of integrated circuits are investigated. In addition, the reliability concerns of millimeter-wave circuit designs and limitations of available algorithms are studied.

2.2 Available algorithms for RLC parasitic extraction

Electrical characteristics of on-chip interconnects are usually modeled using lumped or distributed resistance-inductance-capacitance (RLC) networks. The common algorithm, used in standard CAD tools, is to break the interconnect lengths in many parts and to represent each part as a π / T model, including the series resistance, inductance, and parallel 'to ground' capacitances. The difficulty lies in accounting for the coupling capacitances as well as the mutual inductances in the models. Hence, it is not an easy task to estimate the parasitics, and embed them in the circuit and chip level designs.

The use of EM simulators in practical designs is made possible by innovative diakoptics methods [2.1], where the circuits are partitioned into smaller parts. The overall

circuit performance can be derived from the characteristics of smaller parts and modeling the active devices, transmission lines and the parasitic components in the same environment. Standard tools have been developed to recognize the devices in the decomposition approach, to extract the parasitics, and to include them in the IC design flow. The common methodology to generate net lists from a layout in graphical interface, used by most of the chip-level extractors is shown in Figure 2.1.

From Figure 2.1, there are four main steps to be followed from layout to parasitic netlist generation – (i) layout database creation; (ii) device recognition; (iii) decomposition and estimation; (iv) netlist generation.

(i) Layout database creation: The graphical layouts are used to generate the database in GDS2 formats (acceptable formats for most of the PEX tools). Some of the tools like ASSURA RCX, CALIBRE XRC have embedded software to use the graphical user interface (GUI) directly. Preferably, the layouts need to be layout-versus-schematic (LVS)-ready. The netlist extracted from an LVS-clean layout can be simulated directly using the same platform as that of the schematic netlist without the parasitic components.

(ii) Device recognition: The device-recognition step separates the active devices, the passive devices, and the metal lines (interconnects) from the standard blocks (already modelled p-cells). In this step, already-characterized devices are detected, e.g., MOS devices, NPN devices, capacitors, inductors, resistors, varactors, and transmission lines. Even though, parameterized cells are not used for all of them, LVS tools can still detect active devices after software modifications. After the devices are detected, metal lines are analyzed to detect the device connectivity. Once the netlist without parasitics is created,

net-connectivity database is formed with device positions and detailed connectivity parameters.

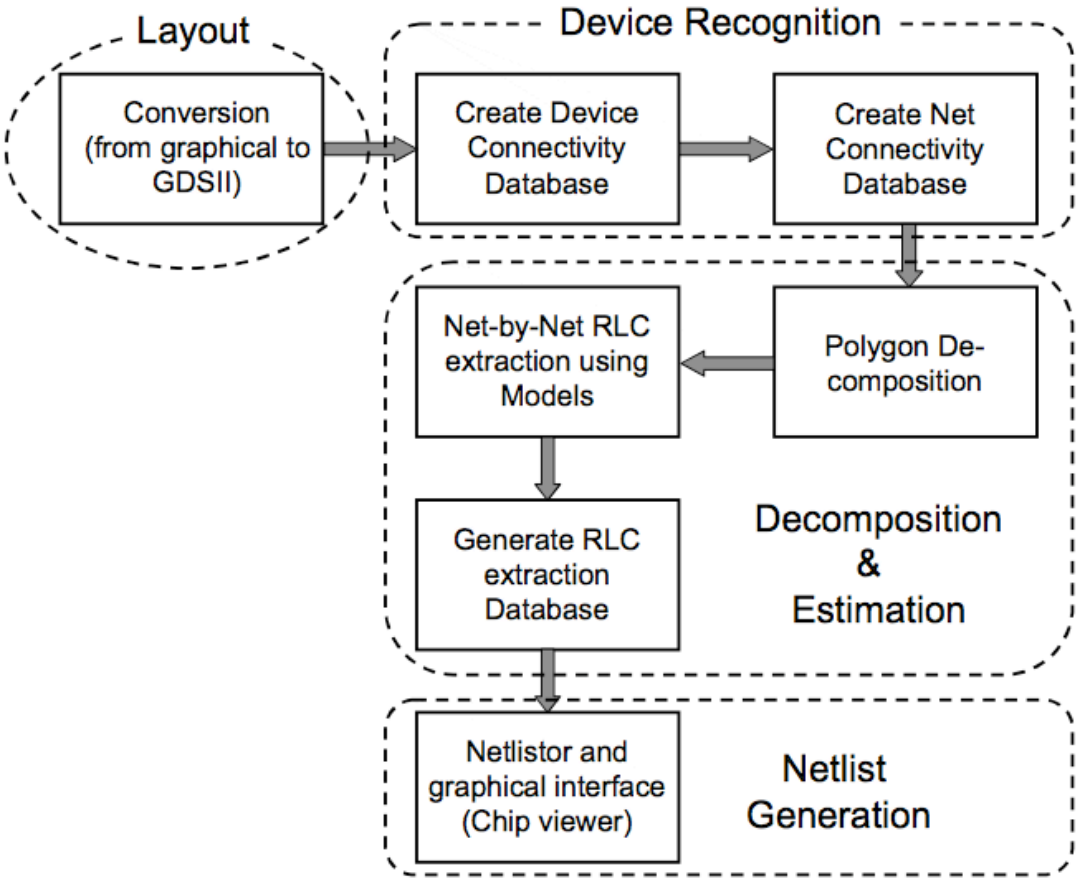


Figure 2.1. The parasitic extraction procedure in an IC design flow.

(iii) Decomposition and estimation: Once the connectivity database is created, the metal lines for connections are decomposed into polygons depending on the maximum fracture length specified. The different geometries of polygons are decided by the capability of extraction tools. There are commercially available parasitic extraction tools that provide the extracted netlists with the corresponding parasitic RLC values. For example, Assura RCX [2.2] is a comprehensive full-chip 3D device-level parasitic extractor, built on the foundation of fast extraction-algorithms. The physics of interconnect parasitics are embedded in the tool as a field solver. The tools are limited by

their training structures, and they may simplify some of the parasitic effects in a multi-layer process. From the embedded models, RLC network for each polygon is extracted from empirical models or tables of values. Mutual inductances and coupling capacitances are evaluated from interactions between polygons. An RLC extraction database is created from those values.

(iv) Netlist generation: From the device netlist and parasitic netlist, the extracted netlist is created in known formats, e.g., Spice and Spectre. Using different interfaces, graphical netlists can be created or separate nets can be studied. The netlists are the outputs of the parasitic extraction tools. They can be simulated in Spice/Spectre platform.

In the following sub-sections, the available algorithms for extracting the interconnect resistances, capacitances, and inductances in integrated circuits are described. Common extraction methods are empirical formulations, numerical methods (e.g. boundary element method), statistical methods (e.g. random walk), 2-D, pseudo-3D and full-3D EM solvers. The full-3D EM solvers are most accurate but suffer from long runtime and the difficulty to incorporate them in chip-level simulations. Thus a non-EM solver based on analytical/empirical models and trained using EM data points can be very effective in terms of runtime and accuracy in chip-level extractions.

2.2.1 Extraction of resistances

The interconnect resistances can significantly influence the circuit behavior by changing the matching conditions as well as reducing the gain, but they also provide stability to the circuits. In the state-of-the-art technologies, low-sheet-resistance aluminum or copper lines are used to decrease the interconnect resistances, but the reduced feature sizes in today's technologies negate the metal resistance reduction.

Convenient methodology for the 'resistance per length' extraction for a metal line is given by the following equation:

$$R = \frac{R_S}{W_{eff}} \tag{2.1}$$

Where R_S is the sheet resistance of the metal line, and W_{eff} is the effective width of the line. W_{eff} is a function of the drawn width, the corresponding electrical bias, and physical bias dimensions. The electrical bias is a technology parameter, and the decreasing effect of the electrical bias on W_{eff} is more significant for lines with smaller widths. Cheesing and fringing effects are considered in most of the resistance-extraction methodologies. The skin effects on the metallization thickness [2.3] can be estimated using EM tools or models that are developed from EM analyses. The substrate resistance of the lossy silicon substrate is another important parasitic component [2.4]. In standard parasitic extraction tools, interconnect resistances are broadly classified as sheet resistances (present for current flowing within conductors) and connection resistances (present for connection layers, e.g., vias and contacts). The sheet resistances vary with temperature variations, process variations, and the current densities.

2.2.2 Extraction of capacitances

Wire capacitances reduce the circuit operating frequency and affect design centering and optimization [2.5]. There are many numerical methods available for interconnect capacitance extraction [2.6], e.g., boundary element method and random walk method. Boundary-element-method-based extraction is accurate but is not suitable for large circuit extraction with large grid requirement. Random walk method [2.7] is used in most of the commercially available capacitance extraction tools, e.g., QuickCap [2.8]. Field solvers

that are based on random walk method may be accurate for large circuits; but they take a very long execution time for the chip-level analog-mixed signal (AMS) and RF circuit extraction. That is why analytical models are used for very fast extraction times, sacrificing the accuracy for complex structures [2.9]. When the tool is proficient, a divide-and-conquer algorithm [2.10] can be applied to extract the net capacitances. The non-EM tools are generally based on analytical models, and hence, they are fast but limited by the complexity of test structures used[2.6].

To summarize, the parasitic tools should be able to extract the intrinsic capacitances (between a conduction layer and the ground), crossover (fringe and plate) capacitances as well as the near-body parasitic capacitances (coupling). The fringing capacitances should be included in the intrinsic capacitances evaluation. The different capacitances, possible in a multi-layer process are shown in Figure 2.2.

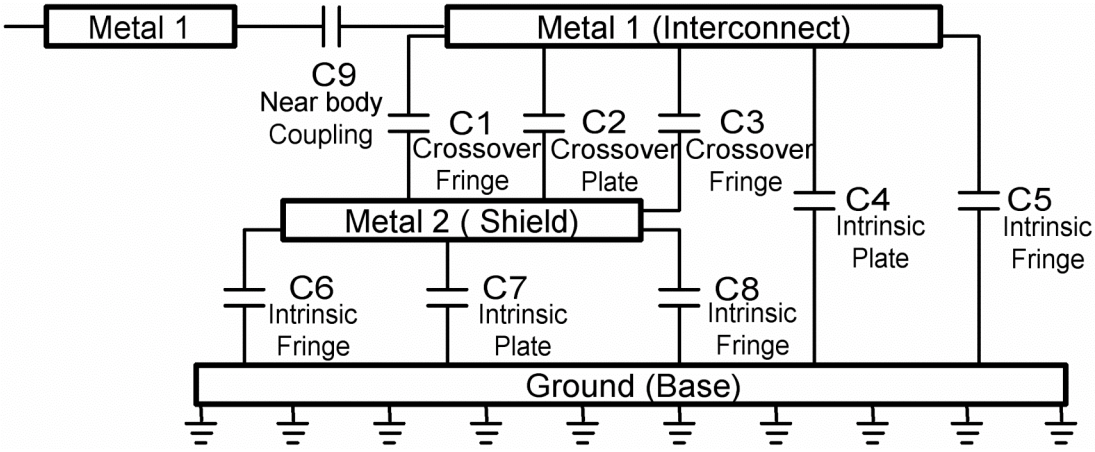


Figure 2.2. Parasitic capacitances for metal interconnects.

Now, there are mostly two different capacitive components- DC and AC. DC capacitances are fixed capacitances whose values do not change with frequencies, and they are usually extracted in most of the PEX tools. AC/RF capacitances are the frequency varying components that are difficult to characterize and solely depend on the

complexity of the structures. Now, at giga-hertz frequencies, any series capacitive structure behaves as a transmission line and has an associated resistance and series inductance values. The series inductance changes the effective capacitance and accordingly the capacitance has a self-resonating frequency (SRF) above which it can no longer act as a series capacitance. But parasitic capacitances are mostly to-ground or to-substrate capacitances, and the inductive effects are not that prominent for them.

2.2.3 Extraction of inductances

Inductances have become important considerations in the design and analysis of on-chip interconnects/parasitics [2.11] for RF/Microwave applications. In some topologies, parasitic inductances are also used to tune the circuit [2.12]. For example, a 50-pH inductance has a reactance value of 18 Ω at 60 GHz, which has to be included during circuit simulations. Complex mesh analyses, combined with different matrix formulations [2.13], are presently used to extract 3D inductances. Quasi-static simulations for inductance extractions are fast [2.14], and they can obtain acceptable results in RF frequencies, but a foolproof numerical-method-based EM simulation [2.15] can give accurate results at multi-GHz frequencies. In MMW applications, line inductances have become important for their high quality factor (Q) and self-resonating frequency (SRF) values. That demands an accurate modeling of on-chip interconnect inductances. In some extraction tools (e.g., QuickInd), the inductance extractions have been simplified using the current-voltage duality, and the matrix elements are modified according to the physics involved. The capacitance delay-time and crosstalk-matrices are replaced by the inductance delay-time and inductance crosstalk-matrices respectively [2.16]. However, statistical or semi-analytic models can be used for specific test structures to save

computation time rather than using a complete 3D matrix solving tool. One such empirical model [2.17] for the self-inductances in a micro-strip configuration (wire with a ground plane) is given by (*W*, *S, T, H* with their usual meanings [2.17]):

$$\frac{L_s}{\mu_0} = 3.71\left(\frac{H}{W}\right)^{0.041} + 0.018\left(\frac{H}{W}\right)^{-0.73} - 3.39\left(\frac{H}{T}\right)^{-0.0006} + \exp\left(-1.89.\frac{S}{H}\right)\left[0.75\left(\frac{H}{W}\right)^{-0.0052} - 0.84\left(\frac{H}{T}\right)^{0.041}\right] \quad (2.2)$$

Similar complex equations can be derived for CPW configurations. But these empirical equations are limited by the physics involved and the nature of equations considered. Also, the coefficients are dependant on the training data used to model, and hence, can have different expressions for different ranges and test structures. It is difficult to predict complex 3-D effects for integrated circuits using polynomial fitting with limited number of terms.

In standard extraction tools, loop and mutual inductances can be extracted with process-stack information and defined ground path. The ground definition is very important for automated tools to decide the loop area given Ampere's law for extracting inductances. Self-inductance can be significant when the design contains nets with long paths. Mutual inductance can be significant when the design contains nets with long paths that are not shielded. Mutual inductance extraction is based on paths (defined in Appendix). The skin effect, which is useful for frequencies above 5-10 GHz, affects the resistance and self-inductance on interconnects in an IC layout design. To find the mutual inductance, it is important to identify the victim and aggressor nets/structures (defined in Appendix) properly. Accordingly, the effects of aggressor nets can be analyzed by enclosing the victim net with the 'tube' of influence using a default radius (up to 500 μm depending on the process) from the center of the victim nets.

In general for chip-level parasitic inductance extractions, two different topologies are available- (i) partial electrical equivalent circuit (PEEC)-based, & (ii) return-limited inductance extractions.

(i) PEEC topology: The PEEC extraction algorithm [2.18] is applied only in user-defined interaction region. User regions are defined as non-overlapping areas on the layout. The user regions are three-dimensional volume elements. Within each user-defined region, partial self-inductances are calculated on all specified inductance nets. Partial mutual inductances are calculated between nets, or portions of the nets, that reside in the same user region but sometimes are not calculated between nets that reside in different user regions to avoid long execution time. This approach is a simple and effective way to manage data size and runtime by processing nets together where magnetic interactions are critical, while isolating nets where the mutual inductance interactions are not considered important. Double counting has to be avoided while scanning each user region in vertical as well as horizontal directions to create two distinct sets of values containing the vertically oriented and horizontally oriented wire segments, respectively. The PEEC method is most appropriate for analog or RF designs where the size of the block or design, or the number of inductance nets, are reasonable.

(ii) Return-loop-limited inductances: In the partial inductance approach previously discussed, the signal, power, and ground nets are extracted explicitly resulting in an inductance matrix that captures all possible magnetic couplings. The return-loop-limited technique generates a sparse matrix of self and mutual loop-inductances. The resulting values capture the inductive effects of the interconnects and maintain a manageable size of the netlist. This topology takes advantage of two properties of high-frequency circuit

behavior. The first is that the power-ground network is well designed with low impedance and is always available as a current return path. The second is that the current returns collapse around the signal lines. Based on these high-frequency properties, the key assumption in the return-limited approach is that the current on a signal line will not return farther away than the nearest power-ground line. By default, the return-limited algorithm automatically partitions the entire layout into non-overlapping interaction regions, or partitions, that are bounded by the nearest power-ground lines. The interaction regions are three-dimensional, like user regions. Within each region the partial self and mutual inductances are computed for the power, ground, and signal lines.

The partial inductances are reduced to loop self-inductances for all the signal lines under the assumption that the signal lines will return current through the nearest parallel power-ground lines. Similarly, the partial inductances between signals wires in the same partition are reduced to loop mutual inductances by considering that the current in a signal wire may also return through a neighboring signal line. The loop inductance values are called return-limited loop inductances. Loop inductance values are usually not considered for, or between, the power-ground lines themselves since their partial self and mutual inductance values are already incorporated into the loop inductance of the signal lines. The final return-limited inductance matrix is symmetric and positive-definite. The latter guarantees convergence during parasitic re-simulation.

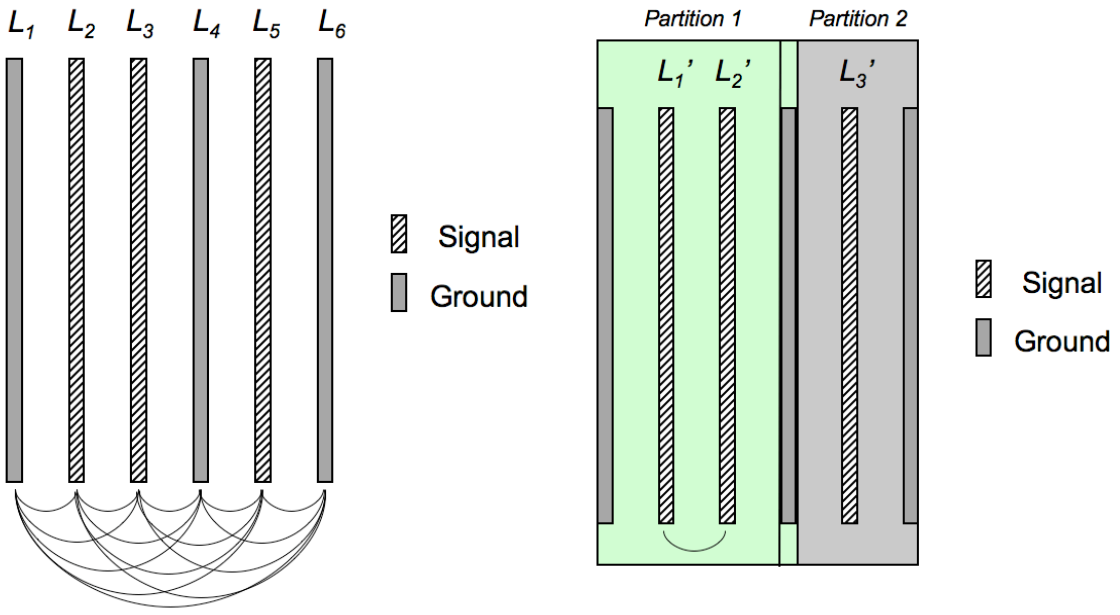


Figure 2.3. The two different approaches to extract inductances.

Figure 2.3 shows the difference between the available two approaches to extract inductances. There are 3 signal lines (striped) and 3 ground lines (gray) shown. From PEEC approach (shown in Figure 2.3a), 5 partial self-inductances and 15 partial mutual inductances are evaluated, and accordingly, equivalent inductances are calculated from equations [2.18]. For return-loop-limited inductance calculations (shown in Figure 2.3b), there are two vertically oriented interaction regions (partitions 1 and 2). Three return-limited loop self inductances and one return-limited loop mutual inductances need to be calculated. Hence, the values of self and mutual inductances reported in the final netlist will vary depending on whether the PEEC or the return-Limited algorithms are used. Further, the number of parasitic inductances and their values usually vary depending on whether automatic partitioning is used, or whether 'User Regions' are specified [2.2]. In usual layout scenarios, mutual inductances should be avoided wherever possible by maintaining spacing between RF lines.

2.2.4 Broadband interconnect model

At low frequencies, current flows uniformly throughout the wire cross-section. For a single wire in free space, current tends to crowd toward the surface of the conductor at higher frequencies (i.e., skin effect). The current distribution can be further modified due to the proximity effect, which is dependent on nearby conductors and the relative phases of the currents within the wires. By default, each line segment is represented by a resistor in series with a self-inductor. When high-frequency effects are considered, a ladder network (Figure 2.4) comprised of frequency-independent elements [2.19] can be used to model the broadband frequency dependent behavior of each line segment. As frequency increases, the resistance of a wire increases while the inductance decreases. A single parasitic netlist with ladder networks is valid from DC to 50+ GHz.

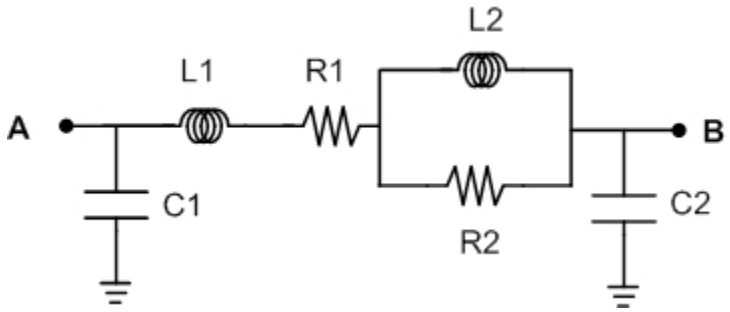


Figure 2.4. Broadband interconnect model.

The value R1 and the sum (L1 + L2) are the resistance and partial inductance values at DC, respectively. As frequency increases, the total resistance of the ladder network increases as the inductor L2 starts to electrically open, and more of the current flows through the resistor R2; conversely, the total inductance tends to decrease for the L2 portion. Thus, ladder networks can be used to model the skin effect of a single conductor segment. Further, in the return-limited algorithm, a heavily doped substrate can be modeled implicitly by accounting for the high frequency eddy current losses. The

substrate effects are discussed in the next sub-section. The capacitances are included as C1 and C2 and their value of (C1+C2) can be considered as the DC capacitance, combined with AC component. The capacitance variation is relatively small compared to resistances and inductances.

2.2.5 Substrate parasitics

In heavily doped substrates, magnetic fields generated by interconnects penetrate into the substrate and generate eddy currents, altering the effective values of interconnect inductances and resistances. With the increasing complexity of mixed-signal and RF designs, and with the decreasing feature size of device technologies, characterization and back annotation of parasitic coupling through the substrate has become a key issue in eliminating problems and iterations from the design of new circuits. In some commercially available PEX tools, the substrate parasitic extraction is integrated into RLC extractions to develop a more thorough model of the substrate. The substrate network is shown in Figure 2.5.

The physical layout and technology descriptions are generally used to generate a macro-model of the substrate, featuring resistive bulks and wells, linked by junction capacitances. The intrinsic capacitances of highly resistive substrates need to be incorporated into the model when needed, according to the maximum frequency of operation.

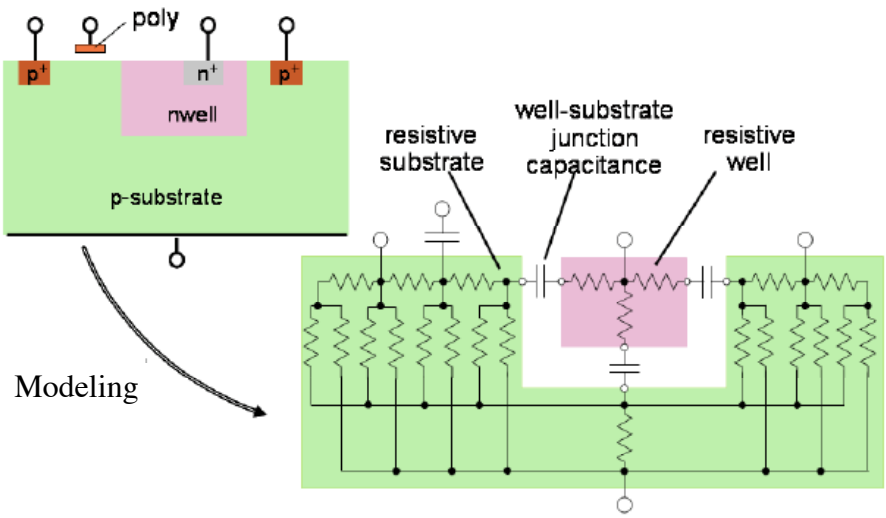


Figure 2.5. The substrate network.

Ideally, a three-dimensional substrate model needs to be extracted. The X Y plane of the layout objects gives two dimensions of the substrate model, and the third dimension is given by the technology description. The substrate netlist that contains the electrical model of the substrate including parasitic capacitors and resistors can be generated from this three-dimensional model. The substrate netlist can be included in the design as a sub circuit to more accurately simulate the entire design.

2.3 MMW circuit applications and parasitic sensitivities

Modeling of parasitics and verification of the model are both essential for a reliable circuit design approach. The usefulness of the tools based on non-EM solving methodologies is dependant on a verification routine that has to be fast, automated, and systematic. The basic CAD design flow is shown in Figure 2.6a. A CAD design tool is utilized using the modeled devices for different circuit topologies. Parasitic extraction comes into place between design-to-layout creation and the design optimization including the extracted parasitic components. The significance of the verification of extraction

methodologies in an integrated system design flow is explained in Figure 2.6b. The design reliability is directly dependent on the extraction accuracy of the CAD tools used to estimate the parasitics that degrade the overall device, circuit, and system performances.

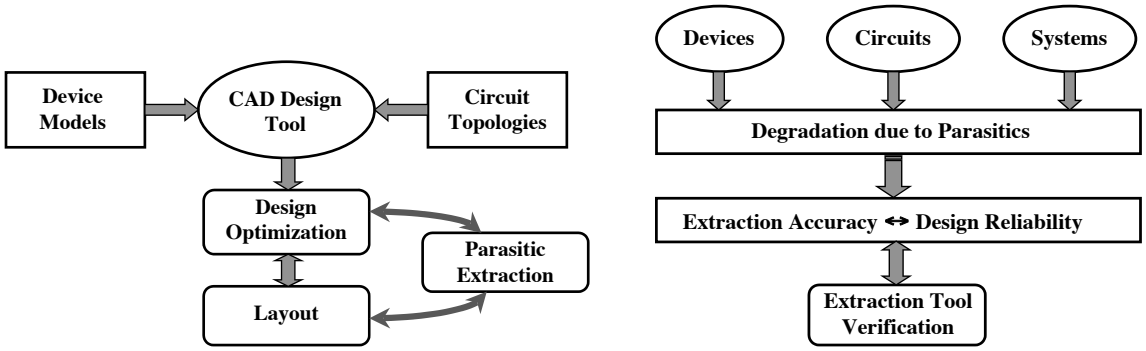


Figure 2.6. (a) CAD design flow; (b) the significance of verification for the extraction methodologies.

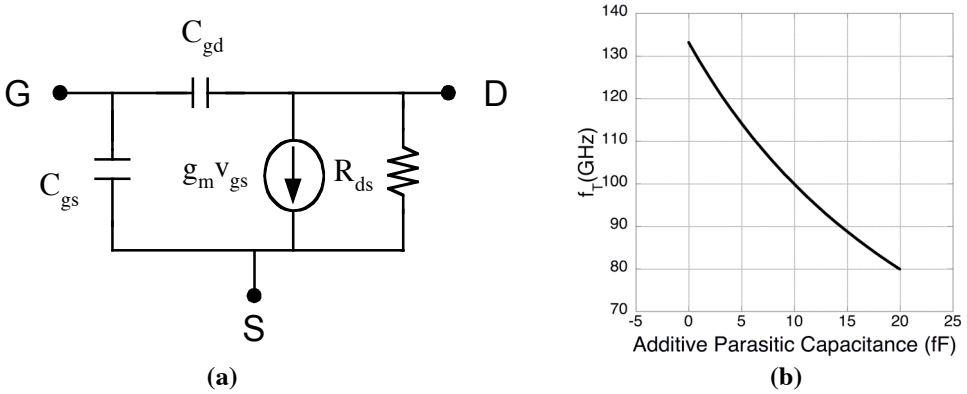
2.3.1 Device- and circuit-related issues with examples

The design of millimeter-wave integrated circuits cannot be optimized until the effects of the wire parasitics are taken care of. It is a misconception to minimize every parasitic possibility to optimize the designs, since not all parasitic effects denigrate the circuit performance. Also, for a reliable design, parasitics are sometimes the key components to stabilize the circuits and to reduce the inconsistencies from process variations. Parasitic inductances and capacitances do not always add on to the same effects. They may oppose each other, and a precise layout optimization can neutralize and reduce their effects.

Let's consider the effects of parasitics in an NMOS device [2.20]. In a very simplified model, the unity gain bandwidth f_T [2.20] is given by equation [2.3].

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{2.3}$$

Where g_m is the forward conductance (derived from dc conditions) and C_{gs} is the gate-to-source capacitance. The model considered is shown in Figure 2.7a. The effects of the additional parasitic gate-capacitance on f_T can be traced as in Fig 2.7b for an NMOS device with g_m= 25.1 mS and C_{gs}= 30 fF.



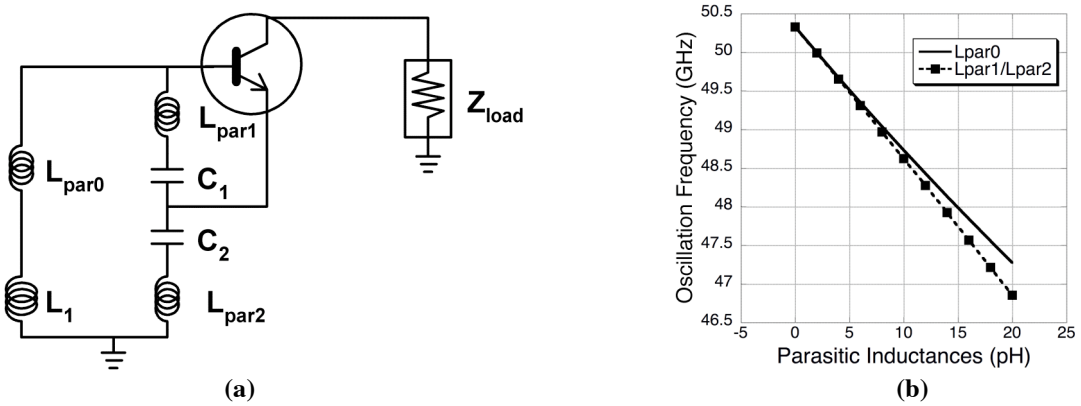
(a) **(b)**

Figure 2.7. (a) The simplified NMOS model; (b) the effects of parasitic capacitance on f_T.

RC delay is very important [2.11] in high-speed digital circuits for the reliability of the circuit operations. However, in MMW designs, inductances are more critical. To understand the role of inductances, let's consider a Colpitts oscillator [2.21] as shown in Figure 2.8a. The additive inductances are identified as L_{par0}, L_{par1} and $L_{par2.}$ The frequency of operation in absence of parasitics is given by:

$$f_0 = \frac{1}{2\pi\sqrt{L_1 \frac{C_1 C_2}{C_1 + C_2}}} \tag{2.4}$$

The independent effects of these inductances are shown in Figure 2.8b. The values of the tuning elements are assumed as: L_1= 0.15 nH, C_1= 100 fF and C_2= 200 fF which gives f_0= 50.33GHz. (Calculations simplified by assuming small change of frequencies). The frequency is shifted by more than 5% for parasitic inductances as low as 20 pH.

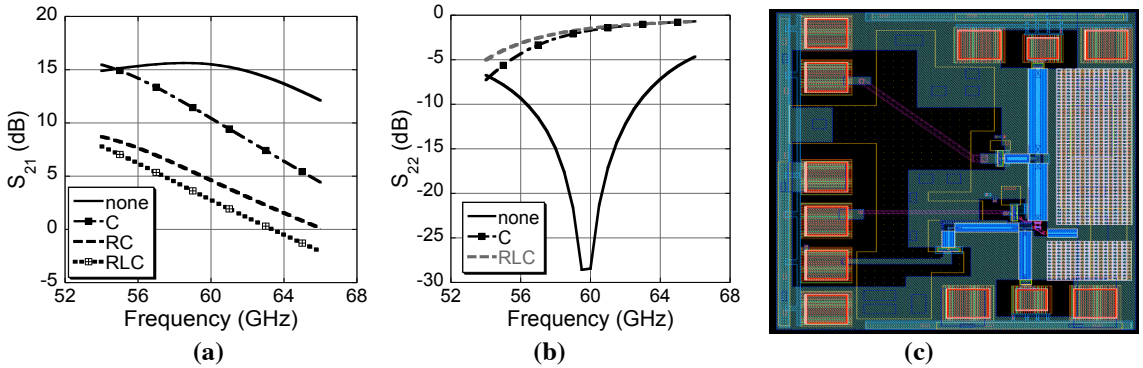


(a) **(b)**

Figure 2.8. (a) Schematic; (b) the effects of parasitic inductances on a Colpitts oscillator.

Therefore, it will not be an understatement that the parasitic effects need to be considered accurately for any parasitic-optimized design for millimeter-wave wireless applications [2.22]. The higher demands of accuracy can be explained from the fact that a capacitance of 20 fF and an inductance of 20 pH can create shifts at 60 GHz as much as a 1.2-pF capacitance and 1.2-nH inductances can do to a circuit operating at 1 GHz. The capacitive and inductive effects, being additive in several cases, can degrade the circuit performances a lot more than parasitic component at a single node can do. It can also cause signal integrity problems.

The effects of the layout parasitics are prominent in oscillators, but it cannot be neglected in other front-end blocks of communication systems e.g. amplifiers, mixers at millimeter-wave frequencies. The effects on the performances of a single-stage 60 GHz SiGe-amplifier are considered in Figure 2.9 with different parasitic extraction routines for different nodes. The layout of the amplifier is shown in Figure 2.9c. The effects of capacitances are found to be most significant for the matching conditions, and the gain is significantly reduced for the layout parasitics. The layout parasitics also modify the bandwidth by affecting the lower and higher frequencies, in a different fashion.

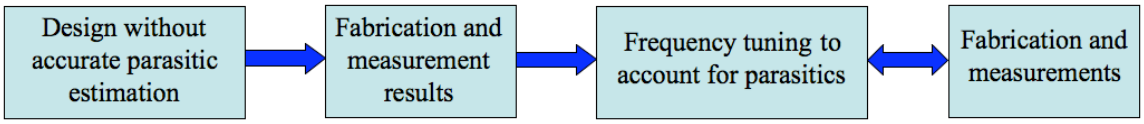


(a) **(b)** **(c)**

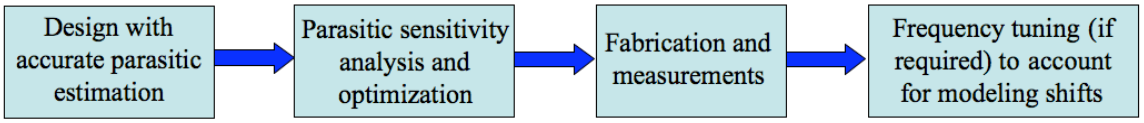
Figure 2.9. Effects of parasitics on an amplifier with different extraction routines :(a) gain (S_{21}); (b) output matching (S_{22}); (c) the layout of the amplifier.

2.3.2 Why estimation and optimization?

There are two different approaches to deal with parasitics in integrated circuit design flow. The standard approach is to extract some of these components and then from the measurement results, re-tune the circuit to meet the specifications in consecutive fabrication runs. The other approach (the one proposed in this work) deals with extraction and optimization of parasitics and accordingly, redesigning the circuits/systems to reduce parasitic sensitivity. The first approach drives the designer to tune the circuit at higher frequencies and expect a certain percentage shifts. The proposed approach suggests an initial layout with estimated parasitics and recursive centering of the design according to the sensitivity analyses of parasitics. The shift expected in second approach is much lower than the first approach, and hence, it is more reliable considering the process variations. Also, the second approach relies on predicting and reducing the parasitic shifts with accurate estimation and optimization of parasitic components in the design flow. The different topologies are described in Figure 2.10a and Figure 2.10b respectively.



(a)



(b)

Figure 2.10. The topologies for MMW circuit design including parasitics.

There are three main issues to be considered to compare these two topologies.

(i) Number of design passes: If parasitics are not extracted properly, it is very difficult to tune a circuit operating at frequencies higher than 10 GHz. For most of the applications, whether it is a narrow-band circuit or a wide band circuit, it has to be centered properly. The bandwidth requirement may vary from 1% to 100% or more depending on the application. Now, for example, to design a 70 GHz oscillator with 1 GHz tolerance, using first approach, the frequency is centered at 77 GHz assuming 15% shifts from device models and parasitics. But the parasitic effects turn out to be more than expected and the circuit oscillates at 66 GHz. Then it is re-centered at 82 GHz to cover the difference. In the consecutive run, it works at 72 GHz, still not meeting the specifications. In this design approach, it will be very difficult to attribute the shifts to only parasitics and not device model. So one needs more than two runs to center the design in this case following the first approach (Figure 2.10a).

But using the second methodology, parasitic variations are reduced to 7% (say) from 15%, and all the parasitics are optimized according to their sensitivities. Hence the design is working at 70 GHz including all the parasitic effects. In this process, the non-reliability

factor due to parasitics is also reduced. Say, if the oscillator gives a measured performance of 72 GHz, it is easy to identify whether the shift is due to modeling inaccuracies and accordingly, the circuit can be redesigned and centered in the second run. So, parasitic optimization and accurate estimation can reduce the number of passes from 3-4 to 1-2. To meet the competitive industry requirement and ever-changing standards, the reduction of design passes is very important, and it can save years of development. Also, the order of improvement depends on the type of circuit. For tuned circuits like oscillators, narrow-band amplifiers accurate modeling/estimation of layout parasitics is a must. Hence these two topologies signify the difference between tuning using multiple runs and accurate estimation of parasitics using minimal runs.

(ii) Optimization and choice of circuit topology*:* Design centering including parasitics is a must for meeting the standards of commercial MMW applications. The reliability and performance concerns that are originated from interconnect parasitics and device model deviations demand a layout optimized for parasitics and eventually, an optimized design including all the layout parasitics. Also, the choice of design topology should not be only based on design specifications but the associated parasitics need to be weighed. For example, in this work, for SiGe-HBT oscillators, neg-R oscillators are found to give better (parasitic) performances compared to cross-coupled oscillators. The reason is lower parasitic deviations (5-10%) in neg-R oscillator compared to higher (20-30%) shifts in cross-coupled topology. In case of neg-R oscillator, the oscillation frequency depends mostly on the active device models. Cross-coupled oscillation frequency depends partly on the device parameters and mostly on the tuning elements (inductances, varactors etc). Hence, if for some process, the active device model shifts

are more than parasitic deviations, cross-coupled topology may be a better choice, given both gives comparable performance excluding the parasitics.

(iii) Failure due to parasitics: The worst-case scenario happens when the circuit or system fails just for undermining parasitics. One example may be when the designer designs the circuit close to the technology limits, and the active device operation cannot provide the functionality in presence of parasitics. Say, we are designing an oscillator at 80 GHz for 120 GHz f_T process using a certain topology. Without estimating parasitics, the oscillator is designed at 100 GHz following the first approach (Figure 2.10a) given a 20% variation, but in actual process the f_T reduced to 110 GHz and the oscillator did not work. On the other hand, if the parasitic shift is minimized to 10%, the oscillator without parasitics needs to be designed at 90 GHz, and it has a better probability of oscillation. In case of failure, it just adds to the number of runs because it does not give any insight of why the circuit did not work. So if the oscillation frequency shifts, it helps the consecutive tuning but not otherwise.

Similarly, for a narrowband circuit, parasitics can ruin the circuit performance. For example, consider the amplifier studied in previous sub-section. The layout and schematic of the amplifier are shown in Figure 2.11a and Figure 2.11b respectively. Looking at the input and output matching circuits of the layout, the capacitance values required are 216 fF and 120 fF respectively. Now in the layout connections, if long lines are included in series with the capacitance to ground, the matching shifts will be fatal for the amplifier gain and matching. Also the parasitic inductance of the MIM capacitor will contribute to the inductances Lp1 and Lp2. The effects for these two inductive elements

to the matching shifts are shown in Figure 2.11c and Figure 2.11e. The effects on the amplifier gain are shown in Figure 2.11d.

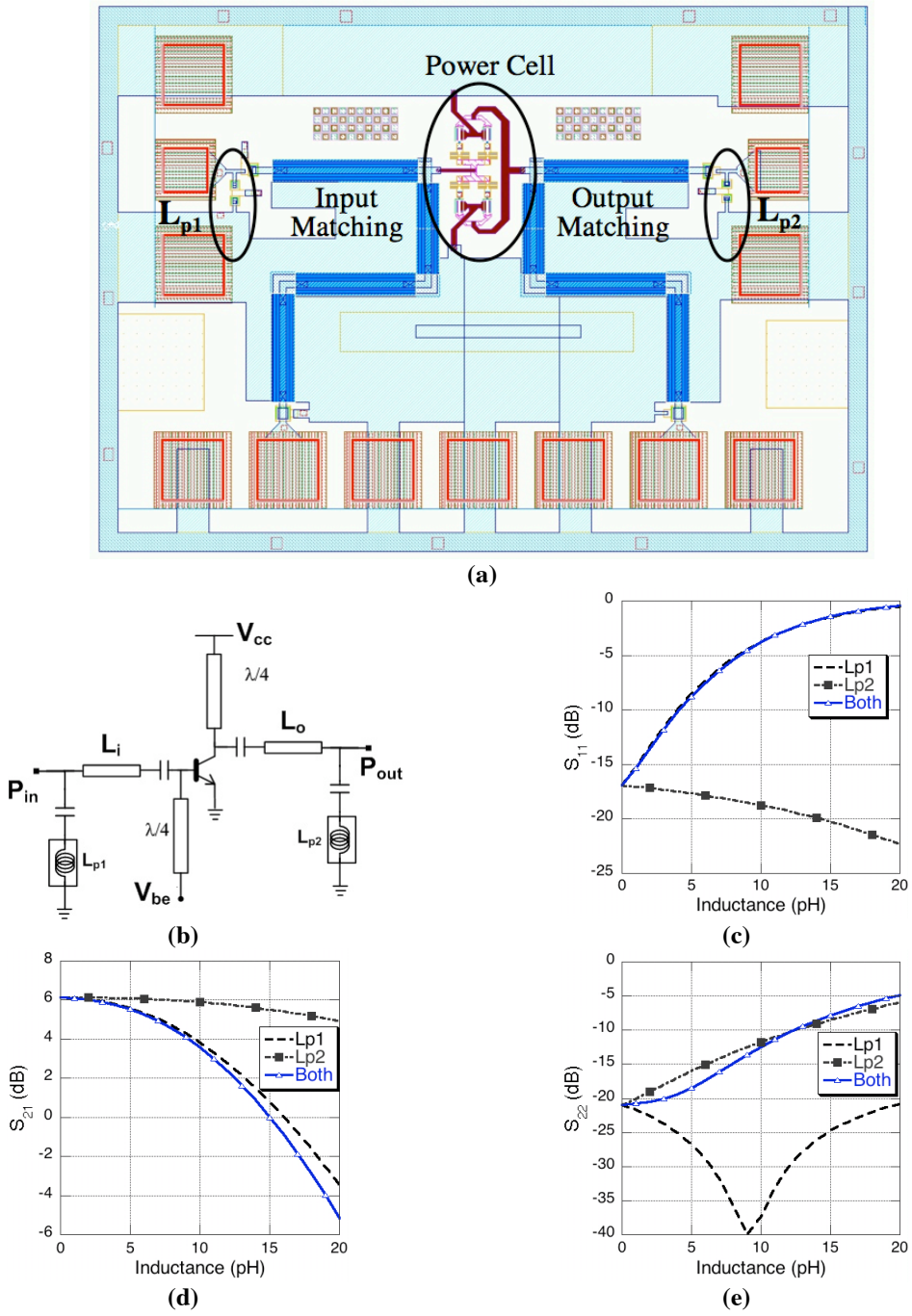


Figure 2.11. (a) The layout; (b) the schematic; (c) effects of parasitics on input matching (S_{11}); (d) effects of parasitics on forward gain (S_{21}); and (e) effects of parasitics on output matching (S_{22}) for the power amplifier.

Now, consider the VCO-Mixer integration with power amplifier (PA) in a super-heterodyne architecture as shown in Figure 2.12. The VCO and mixer targeted specifications are as shown in the figure.

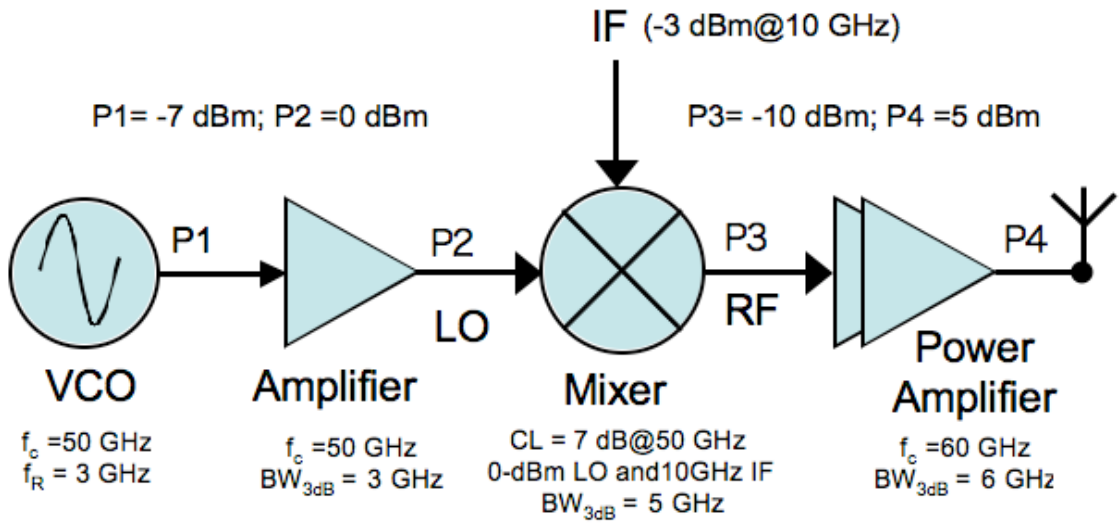


Figure 2.12. The VCO-Mixer-PA system.

Say, the center frequency of VCO is shifted to 49 GHz with -10 dBm output power a deviation from targeted specifications of 50 GHz with -7 dBm output power. The amplifier being a tuned amplifier gives 2 dB less gain than targeted. Thus LO power reached is 5 dB less than desired. Even while using a wideband VCO, the frequency shift can be compensated but the power degradation may be more than 6 dB. Thus the mixer will get 5 dB lower LO power and accordingly, can give a lower output power at RF port. That will reduce the PA output power. If the frequency cannot be shifted to mixer range, the mixer conversion roll-off will affect the conversion characteristics by as high as 2-6 dB (given, narrowband mixer). That decrease can create a 6-12 dB lower input power to PA and can significantly reduce the system performance. Hence, if the VCO frequency shifts by 2% due to unaccounted parasitic effects, the system fails to meet the specifications.

For a broadband circuit, the maximum operating frequency is the main performance parameters. For opto-electrical systems, the frequency in digital PRBS data transfer may vary from 100 MHz to 50 GHz, and hence, broadband models for parasitic components are required. Though the parasitic extraction is not so significant as in narrow-band circuits, the optimization of device parasitics is a necessity to operate the devices in their limits.

2.4 Literature survey

With increasing operating frequencies of digital and analog-mixed-signal circuits, the CAD tools are improved to estimate the wire parasitics. Still due to the inaccuracies of PEX tools in the millimeter-wave domain, the standard procedure is to use measurement results of active and passive devices to characterize interconnect parasitics around devices and to retune the circuits from measurement results of the fabricated circuits. But, the initial design of the circuits should be done including already modeled intrinsic and extrinsic parasitics around the devices. The proposed methodology (described in the previous sub-section) is better than the standard approach for the parasitic sensitivity analysis and the possibility of embedding neural-network-based interconnect models in RF design environment.

Some research has been performed for parasitic aware designs [2.22] in circuits operating at frequencies 1 to 10 GHz. But a detailed analysis of the role of parasitics in high-frequency systems is still missing in literature. The recent trend of using sub-100 nm CMOS circuits demands an accurate characterization of parasitics. Since with decreasing size of transistors, the parasitic capacitance is quite comparable to the active device

(MOS) capacitance, thus, limiting the performances. In CMOS processes (like 45 nm, 65 nm and 90 nm) that can be used up to 100 GHz, the accurate extraction of parasitics and embedding those RLC networks into design environment become very challenging tasks [2.23]. In digital domain, the interconnect delay due to parasitic effects becomes more dominant cause of delay than the gate switching delay for these processes. The increased importance of interconnect delay at smaller geometries, it is imperative to the success of sub-100 nm designs to manage parasitics with a stress of accuracy and optimization. In recent years, CAD tools are improved to incorporate EM-trained analytic/empirical models [2.24, 2.25] for capacitance and resistance extractions for interconnects. Some automated extraction tools for RC extractions are implemented [2.26]. Still now, very few tools are trained to extract inductances of the signal lines. But with decreasing feature sizes, the impact of parasitic inductances can no longer be neglected [2.27]. Also, interconnect parasitics need to be accounted in an analog design optimization environment for their impact in deep-submicron high-performance designs [2.28]. Hence, it is really important to understand the role of estimation and optimization of parasitics in high-speed digital as well as high-speed RF and MMW circuits.

2.5 Summary

The standard methodologies to extract resistances, capacitances and inductances in an IC environment are investigated. The shortcomings of commercially available parasitic extraction tools are explained, and the importance of extraction of parasitic inductances is studied with circuit examples. The significance of the verification of existing extraction methodologies in an integrated system design flow is described. The role of parasitics is explained using simple device and circuit examples. The possibilities of failure from

parasitic components are demonstrated for a power amplifier as an example of circuit and a transmitter at 60 GHz as an example of system. The proposed approach to predict and reduce parasitic shifts is compared to the standard approach to account for layout parasitics. Finally, the literature survey is presented to explain recent interests in understanding the parasitic effects in an IC design flow.

Chapter 3

Parasitic Modeling and Extraction-Verification

3.1 Introduction

The interconnect parasitics need to be estimated accurately and effectively before the systematic design and layout-optimization steps. It is difficult to implement a chip-level PEX tool that can estimate resistances, capacitances and inductances, with the accuracy of 3D EM-solvers. Therefore, the extraction methodologies need to be verified with an EM-solver or measurement results. Manual layout extractions, after identifying major parasitic components from a sensitivity node analysis, may prove to be more accurate than an extensive parasitic extraction for all the nodes in stand-alone MMW circuit layouts. In this chapter, the verification procedure for PEX tools are demonstrated in an automated fashion, and a neural-network-based methodology is presented as an alternative to standard PEX tools for selected applications.

The objectives of this chapter are:

- To develop an automated methodology to verify the parasitic extraction (PEX) tools, and to understand/verify its impact on the modeling of layout parasitics.
- Apply the automated methodology on functional circuits, e.g., ring oscillators.
- To develop an alternate model to available analytical models and to implement that model in accordance with the decomposition approach.

- To develop a parasitic benchmarking procedure using interconnect models for MMW circuits, e.g., cross-coupled oscillator.

3.2 Automated extraction and verification

The first step for studying the effects of parasitics on devices, circuits, and systems, is to standardize the parasitic extraction tools. In this work, a verification methodology has been developed using commercially available PEX tools, and the approach is proposed for the developed neural network-based models. Some part of this work is performed as a co-operative effort between Georgia Electronic Design Center (GEDC), Georgia Institute of Technology, Atlanta, USA and IBM Corporation, Essex Junction, Vermont, USA.

3.2.1 Verification of the algorithm

The automated layout-generation methodology is demonstrated for complex passive structures in a multi-layer process. Different ring oscillator with varying passive delay structures are generated using the same algorithm and later used for verification of extraction methodologies using a 90 nm CMOS process.

3.2.1.1 Verification using passive structures

A set of multi-layer passive structures is used to verify the tools. Cross-sections of one such set is shown in Figure 3.1a-3.1l. Since, a set of simple passive structures is used to account for modeling the parasitics, complex structures need to be used to verify the modeling concept. A silicon-based seven-metal-layer RF process is defined in EM-solver for extraction and modeling purposes. The cross-section of this process is shown in Figure 3.1m. The process has five thin metal layers (1M1, 1M2, 1M3, 1M4 and 1M5). The two thicker metal layers are defined as 2M1, 2M2. The passive structures are laid out

using a meander line topology (shown in Figure 3.1n). Figure 3.1p shows a complex meander line with alternate signal and ground layers. This structure includes both vertical and lateral coupling effects.

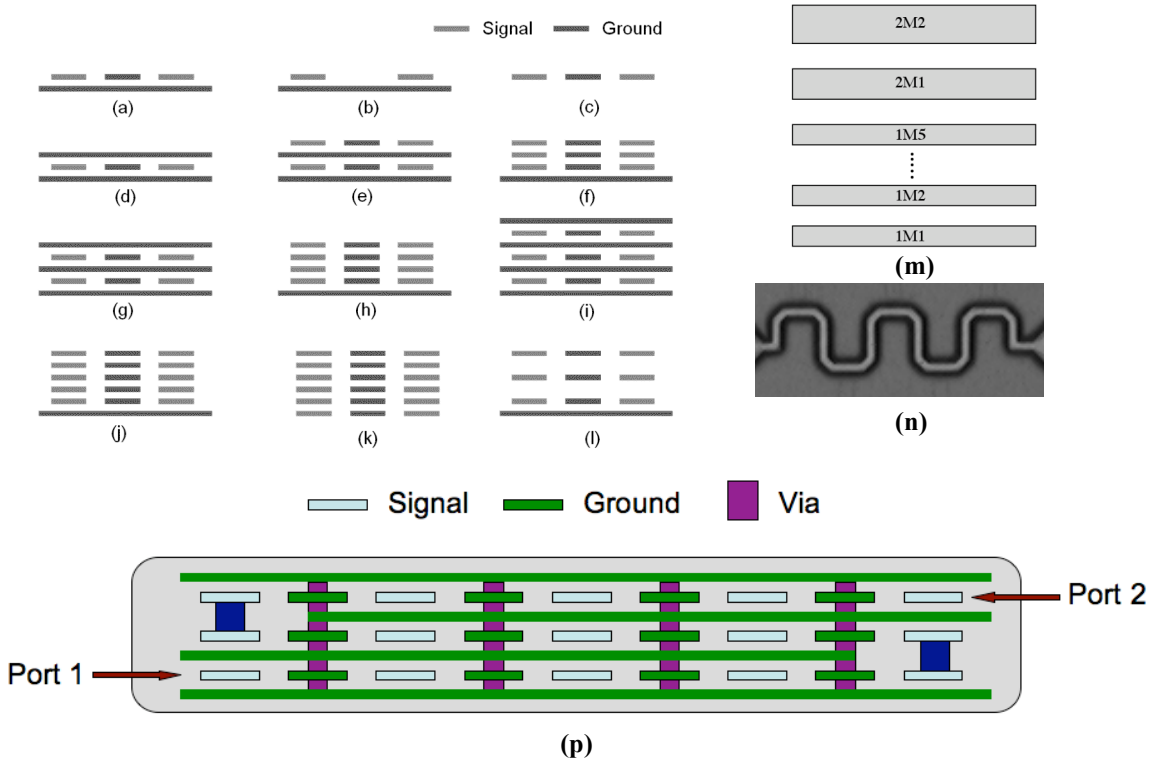


Figure 3.1. (a)-(l) Cross-sections of different multi-layer passive structures; (m) the metal stack; (n) die photo of an example of the meander line structures (top metal with 1M1 ground) and (p) the cross-section of a complex meander line structure.

One such set of structures is described in Table 3.1, and the capacitance comparison results from EM and non-EM tools are summarized in Table 3.2. The test cases T1-T10 as described in Table 3.1 are meander-line structures in different metal layers with repetitive layouts similar to that shown in Figure 3.1p. The poly-silicon (poly) layers are included as ground planes to estimate the gate parasitics that are very important in the characterization of CMOS devices. It is evident that the extractions of the non-EM parasitic extraction tools, named as Tool A, B, C, D and E, give different values for the same structures. The coherency with EM tools depends on the complexity and topology

of the test structures. For example, the structure T6 is designed to include the edge coupling effects that are considered in Tools C, D and E. But, Tool A overestimates the edge coupling, whereas Tool B cannot estimate the same effect. This proves the insufficiency of the analytical models developed from test structures. In addition, the analytical models cannot estimate all the complex effects that are included in EM solvers or a neural-network-based methodology.

Table 3.1. Description of an example-set of structures

Structures	Description
T1	Meander line on 1M1, 1M3, 1M5 layers with inter-digitized grounds and ground-planes on poly, 1M2 and 1M4 layers.
T2	Meander line on 1M1 layer with inter-digitized grounds and ground-planes on poly and 1M2 layers.
T3	Meander line on 1M1, 1M3, 1M5 layers with inter-digitized grounds and ground-planes on only poly layer.
T4	Meander line on 1M1, 1M2, 1M5 layers without inter-digitized grounds and ground-planes on poly, 1M2 and 1M4 layers.
T5	Meander line on 1M1 layer without inter-digitized grounds and ground-planes on poly and 1M2 layers.
T6	Meander line on 1M1, 1M2, 1M3 layers with inter-digitized grounds and ground-planes on poly layer.
T7	Meander line on 1M1, 1M2, 1M3, 1M4, 1M5 layers with inter-digitized grounds and ground-planes on poly layer.
T8	Meander line on 1M1, 1M2 layers with inter-digitized grounds and ground-planes on poly layer.

Table 3.2. Comparison of capacitances

Structures	Capacitances (fF)					
	EM	Tool A	Tool B	Tool C	Tool D	Tool E
T1	928	952	958	992	976	963
T2	317	333	329	347	344	346
T3	824	891	917	988	859	836
T4	465	490	473	533	549	487
T5	190	199	190	213	227	204
T6	765	801	721	795	773	776
T7	1213	1285	1125	1215	1222	1240
T8	508	559	516	571	545	536

3.2.1.2 Verification using ring oscillators

The modeling of interconnect structures and the verification of PEX tools involve generation of many test-structure layouts. Hence, an automated layout-generation methodology is needed to minimize execution time. In this work, a layout-generation methodology has been built using Matlab codes and Perl scripts. The block diagram for this methodology is shown in Figure 3.2. This method is useful for the generation of input passive structures for neural network modeling, as well as for the verification of PEX tools using functional circuits.

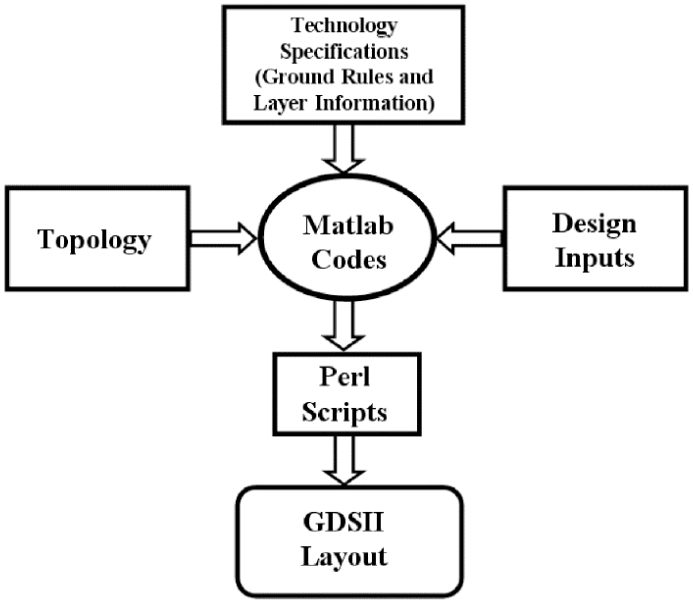


Figure 3.2. The automated layout-generation methodology.

The developed methodology is very fast, and design-rule-check (DRC)-clean layouts for a set of 20 structures can be generated within ten minutes to one hour, depending on the complexity of the layouts. Codes are written in Matlab using Perl scripts, which in turn can be executed to produce layouts in GDSII stream formats. All the codes, used for layout generation consist of two basic blocks- (i) Input section: Here, the inputs for the

layout generation, such as the technology specifications, the design inputs, and the interconnect topologies are included. The ground rules for layouts are also incorporated in the technology-specified file. Thus, choosing a different technology file, the layer information and the ground rules can be modified automatically. Test-structure topologies include definitions of the signal layers and the ground planes as well as the dimensions that are back calculated from the required delay; (ii) Execution section: Here, functions are executed according to the rectangular co-ordinates defining the blocks in different metal layers. Different functions, representing several topologies, are executed in the same code to generate a set of structures. The layout-generator code can also be used to create the test structure layouts, required for training the neural networks, described later in this chapter.

The automated generation technique is illustrated using ring oscillators as examples of functional circuits. Ring oscillators have already been used for technology benchmarking [3.1]. In this work, ring oscillator is used as an example of active circuit, where the parasitic structures, used as delay cells in between inverter stages, can verify the resistance- and capacitance-extraction methodology. The main code (that generates the ring oscillator structures) calls different functions to create the inverter cells, the delay cells for the given number of inverters in the oscillator, the delay required, and the die-space assigned [3.2]. The connections to the rails are made symmetrically, and the pins are placed using proper metal layers. Any advanced parasitic-extraction tool can be used for the parasitic extraction of the ring oscillators if the layout-versus-schematic (LVS) extraction and device recognition steps are performed correctly. Since, the automatically generated ring oscillator layouts are DRC-LVS-clean, the complexity of the Matlab codes

can be reduced using an automated extraction procedure. The parasitic-extraction tools can generate the net-lists in HSpice and/or Spectre format. Spectre is used in the given example. As the final step of the automated testing, the simulator outputs are plotted for different decks/tools. The outputs can be plotted in the same graph, and they can be visually compared to each other as well as with the "gold standard" (EM) output.

The output waveforms for three different statistical variations (best, nominal, and worst case) are shown in Figure 3.3 for a ring oscillator using IBM CMOS 90 nm process. This automated plotting of the outputs gives another dimension to the verification methodology by visually comparing the extraction results. The verification procedure is very fast utilizing an automated approach, and it does not use any graphical interface. For example, the basic flow of layout generation, extraction and output plotting takes less than 10 minutes for a conventional ring oscillator in a 1 GB RAM 900 MHz dual processor computer.

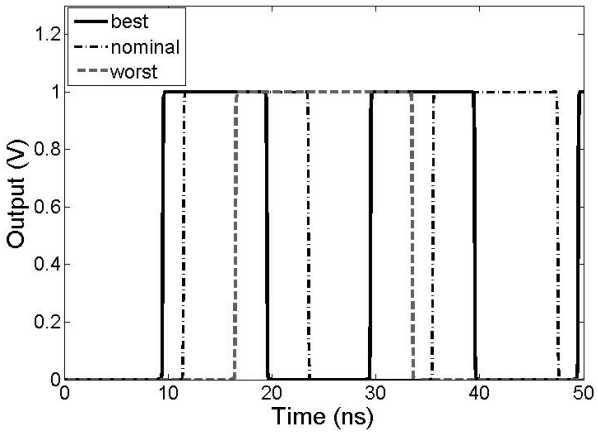


Figure 3.3. Simulated outputs from a ring oscillator for three different parasitic extraction test decks (nominal, best case and worst case).

3.2.2 Measurement results for ring oscillators

The verification procedure using ring oscillators are pictorially represented in Figure 3.4. The initial comparisons are made between commercially available PEX tools, and

the final verification of these tools is performed by directly submitting the test structures generated using Matlab codes in a 90 nm CMOS process. The measurement results derived from more than 80 dies in multiple wafers are used to benchmark the PEX tools and the extraction methodologies.

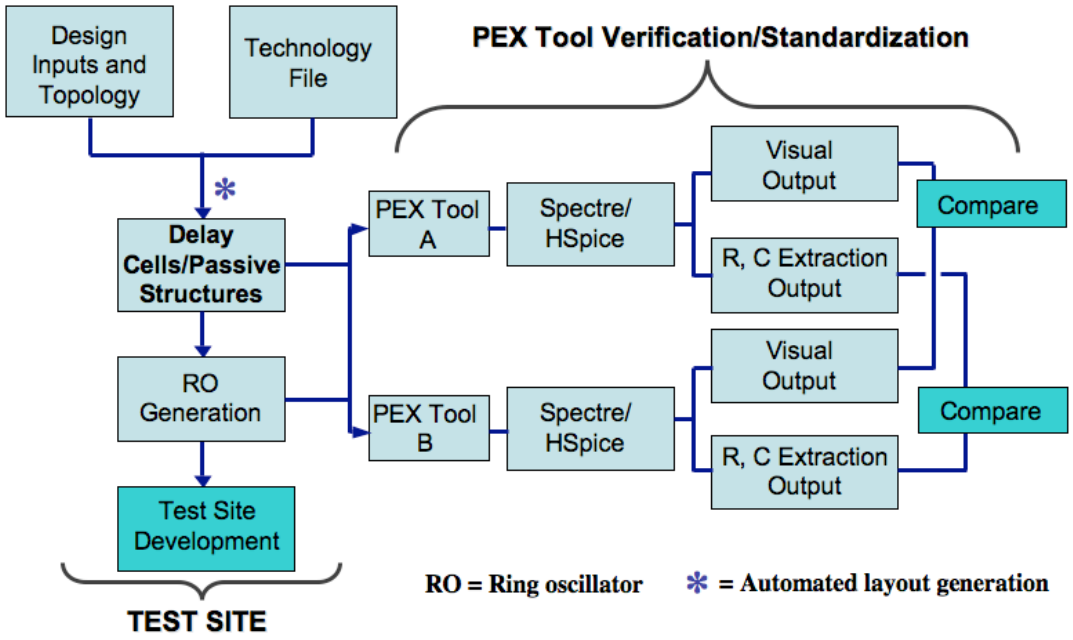


Figure 3.4. The verification procedure.

As shown in Figure 3.4, the design inputs and the topologies of passive structure are fed to the technology-independent Matlab code with the file containing technology information. The passive structures as delay cells for ring oscillators are generated, and later, the ring-oscillator layouts are created using these delay cells. Different PEX tools are used to extract the equivalent RC networks and to determine the oscillation frequencies simulating the ring oscillators, and thus, different extraction methodologies are compared. Usually in Matlab, the ring oscillator extracted netlists are simulated using Spctre/Hspice and visually compared in the same environment. The ring oscillator structures are used to develop test sites for different technologies and thus, utilized for

technology benchmarking. In this sub-section, measurement results obtained from a CMOS test site, consisting of six structures are presented.

Six structures are chosen for fabrication among a set of 20 structures that are used for verification of the tools among themselves. Some of these tools are CalibreXRC, Assura RCX, and STAR RCXT. The chosen six structures consist of the following delay structures:

- RO1 ⇒ Inter-digitized signal lines on 1M1, 1M3, 1M5 with PC, 1M2, 1M4 ground
- RO2 ⇒ A 21.7 μmx0.14 μm 1M1 line for de-embedding active device delay
- RO3 ⇒ Inter-digitized 1M1 signal line with PC and 1M2 ground
- RO4 ⇒ Inter-digitized signal lines on 1M1, 1M3, 1M5 with PC ground
- RO5 ⇒ Signal lines on 1M1, 1M3, 1M5 with PC, 1M2, 1M4 ground (not inter-digitized)
- RO6 ⇒ 1M1 signal line with 1M2 ground (not inter-digitized)

The metal-layer convention is the same as followed in previous sub-sections. In these ring oscillators, the inductive effects are insignificant compared to the capacitive and resistive effects for sub-GHz frequencies. The frequency is further reduced using a divide-by-2^{13} block for simplified measurement procedure. After the divider, a buffer is used to probe the output. The measurement setup is shown in Figure 3.5. The ring-oscillator frequency is not changed by the loading capacitor of the divider-buffer block. The loading cap is around 10 fF that provides >500 KΩ impedance at that node.

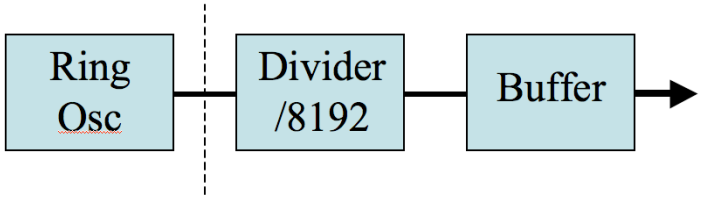


Figure 3.5. The ring-oscillator measurement set up.

The comparison results are summarized in Figure 3.6. The extracted results from two different tools lie between ± 0-6% accuracy compared to measurement results.

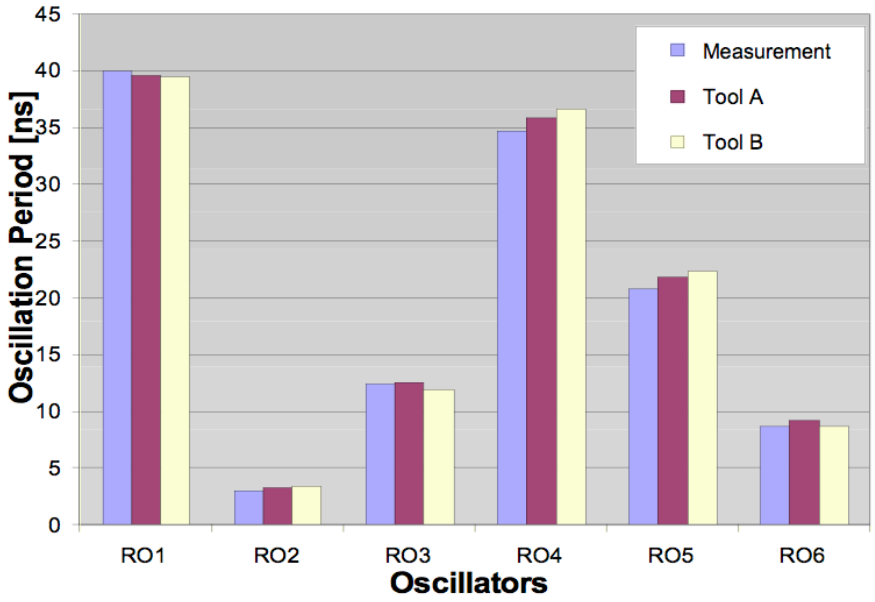


Figure 3.6. The ring-oscillator measurement comparison.

For two specific structures, i.e., RO3 and RO6, the statistical variations of measurement results and the extracted results from PEX tools are presented in Figure 3.7 and Figure 3.8 respectively. Total 87 data points are collected for the ring oscillators. For these cases, Tools A, B and C are within the $\mu \pm 3\sigma$ limits. For RO3 and RO6 structures, Tool A and Tool B give most accurate values respectively. Structure RO3 consists of both lateral and vertical coupling whereas structure RO6 has mostly vertical coupling. Hence, all three tools are found to underestimate lateral coupling effects as evident from

the difference between the frequencies in RO3 and RO6. For RO3, Tool B is close to the upper limit, and hence, it needs to be trained using similar structures for better accuracy.

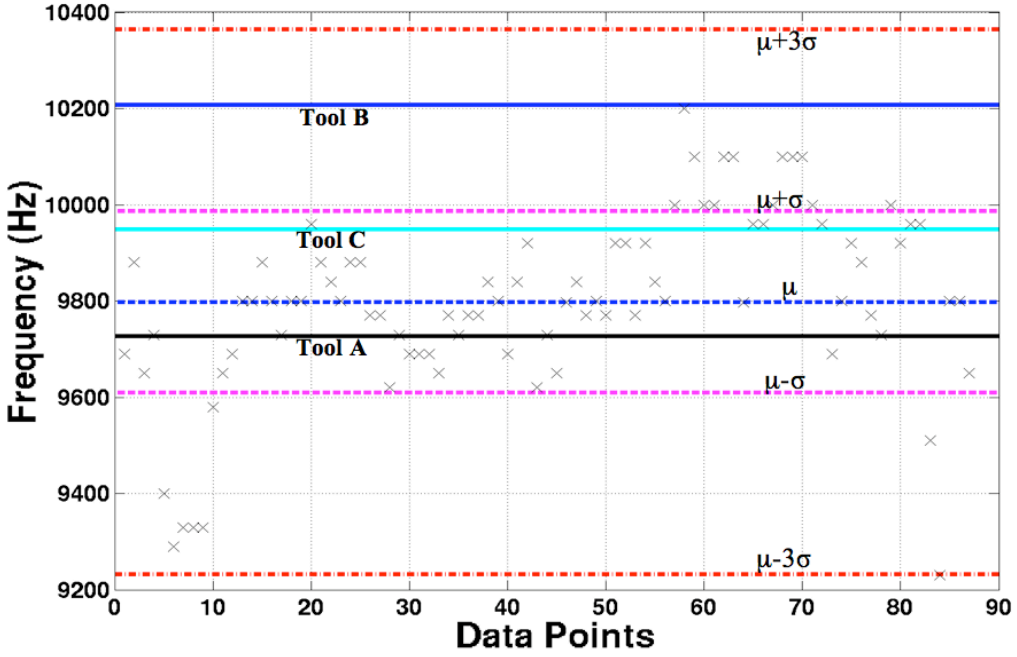


Figure 3.7. The ring-oscillator measurement comparison for RO3.

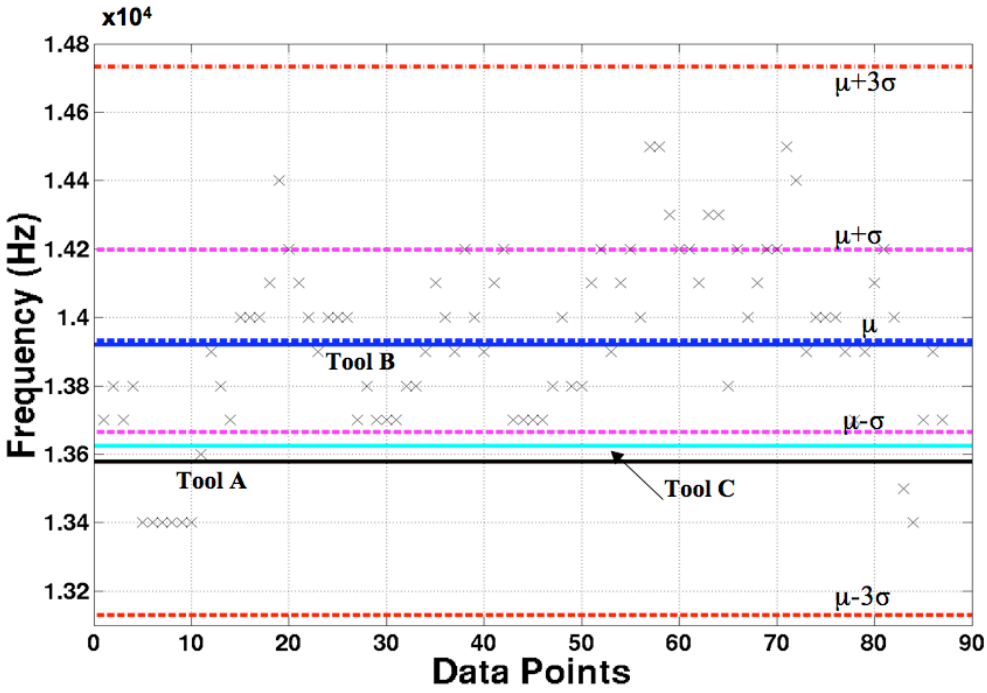


Figure 3.8. The ring-oscillator measurement comparison for RO6.

3.2.3 Applications of this method

The automated layout generation procedure has been used in IBM Corporation to study the effects of fillers and different dielectric definitions for the wire parasitics. It is also used for comparing functional circuits [3.2] varying different process parameters, e.g., layer options and dielectric-stack representations. The fast layout-generation capability enables very fast test-site development and modeling of active, as well as passive structures.

3.3 Modeling parasitics using neural networks

This section describes the application of neural networks to the modeling of parasitics for different interconnect structures. Neural networks have emerged as an attractive technique for modeling complex and non-linear relationships [2.1, 3.3]. Neural networks have the capability to learn arbitrary non-linear mapping between noisy set of inputs (layout parameters) and output parameters (parasitic components).

3.3.1 Description of neural modeling

The type of neural nets, used for modeling in this work, is the multi-layer perceptron (MLP) network consisting of three or more layers, as shown in Figure 3.9. The structure of MLP is well established, and this neural model has excellent generalization capability [3.4].

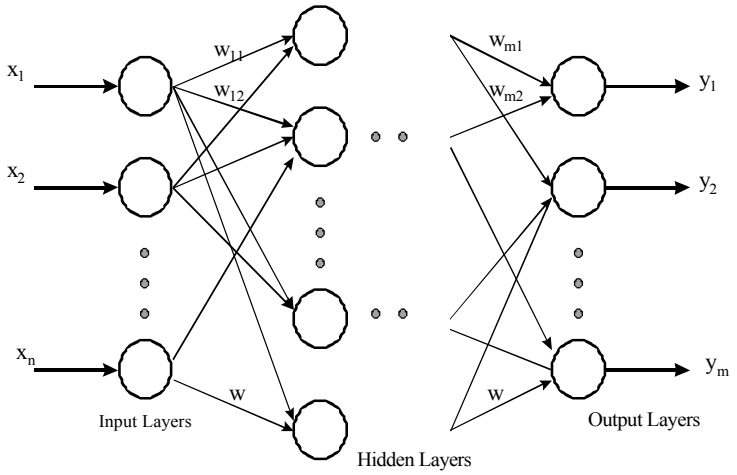


Figure 3.9. Multi-layer perceptron neural-network structure.

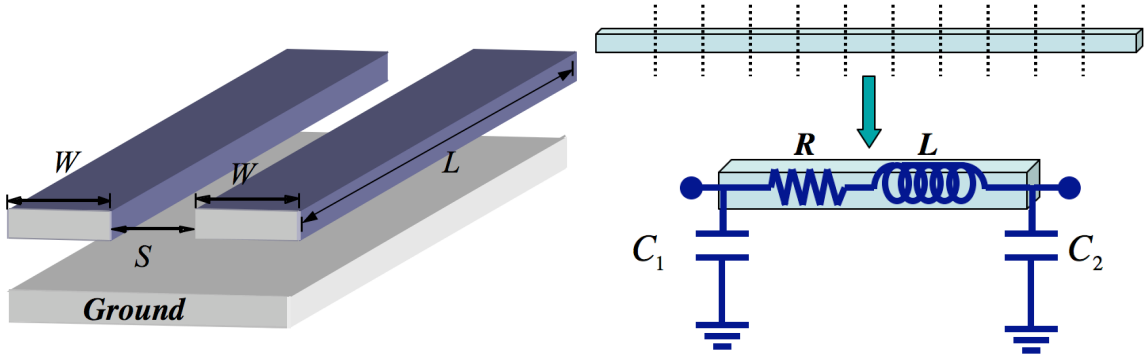
The *x-z-y* neural network structure refers to the number of neurons in the input, hidden, and output layers respectively. The network is typically trained using the error back-propagation (BP) algorithm with a sigmoidal activation function [3.5]. The learning rate determines the speed of convergence by regulating the size of the weight change [2.1]. The model-accuracy parameters such as training and prediction errors [2.1] are evaluated in terms of the root-mean-square error (RMSE).

In this work, an input dataset of 20-40 points is used to train the neural networks in a wide range of width, length, and spacing, wherever applied. Since the accuracy of the model is dependent on the small input dataset, a latin hypercube sampling (LHS) algorithm [3.6] is used to choose the input dimensions from the specified range. The range of input data depends on the complexity of test structures and different metal layers used. The model is trained till the prediction error is less than 3-5% for randomly selected input parameters. The modeling error for dataset, used in training is below 0.1%.

The test structures considered are shown in Figure 3.10a. The effects of other lines are not considered except when coupling capacitance and mutual inductances are modeled. For a line, the S-parameter is symmetric, and hence, it can be modeled as a PI-

network as shown in Figure 3.10b. The equations to estimate the R, L, C_1, and C_2 are given as:

$$R = \mathrm{Re}(-\tfrac{1}{Y_{21}});\ L = \frac{\mathrm{Im}(-\frac{1}{Y_{21}})}{\omega};\ C_1 = C_2 = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega};\qquad (3.1)$$



(a) **(b)**

Figure 3.10. (a) Line in coupling configuration and (b) representation of a single line.

3.3.2 Capacitance modeling

The interconnect capacitances in a complex layout environment can be determined by the superposition of to-ground and coupling capacitances of metal traces, defined in a multi-layer process. One such set of test structure is shown in Figure 3.11, assuming the capacitances in only one layer.

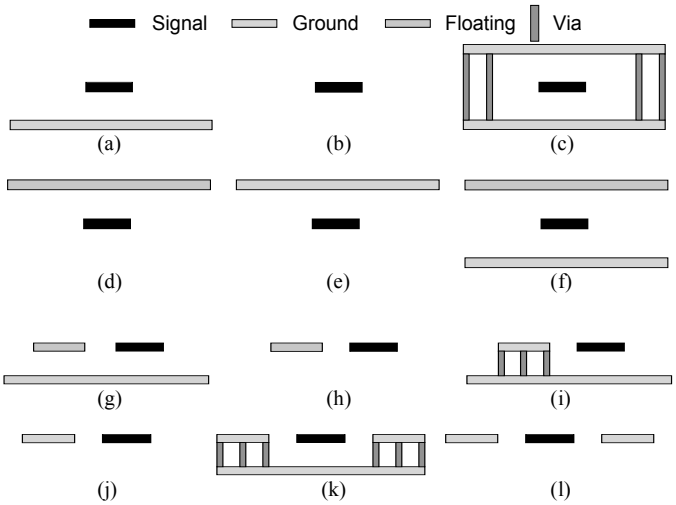


Figure 3.11. The cross-sections of the test structures, used for estimating capacitances.

The process is defined exactly the same as in sub-section 3.2.1.1. From Figure 3.11, the bottom grounded metal layer is assumed to be 1M1 in structures (a), (c), (f), (g), (i) and (k). The signal metal layer chosen for analysis is either 1M2 (metal layer just above 1M1) or 2M2 (top metal layer). The layouts as shown in Figure 3.11 can account for fringing effects, different coupling effects as well as substrate effects.

Neural-network-based models are developed to characterize the capacitances for the selected test structures. A simple parallel-plate approximation is no longer valid for the case, when the metal thickness is comparable to the ground separation. Also, it is difficult to estimate non-scalable interconnect capacitances using analytical models. That is why the neural network models are preferred to analytical models.

The equivalent capacitances are extracted from the simulated Y-parameters [3.7]. To model capacitances in different layers, the electrical design rules (DRC) are satisfied. The ranges and the number of samples are decided from the current carrying capacity and the reliability issues in layouts for the millimeter-wave transceiver circuits. The ranges of input parameters for different cases are summarized in Table 3.3.

Table 3.3. Ranges of dimensions for different metal layers

Dimension	Minimum	Maximum
Width (1M2)	1 μm	20 μm
Length (1M2)	5 μm	50 μm
Spacing (1M2)	0.5 μm	10 μm
Width (2M2)	4 μm	20 μm
Length (2M2)	5 μm	50 μm
Spacing (2M2)	4 μm	20 μm

The width, length, and spacing are of their usual meaning for the interconnects as shown in Figure 3.11. Two separate models are developed for different width (W)/length (L) aspect ratio ranges to increase accuracy. Case I includes W/L ratios from 0.25 to 4,

whereas case II includes the case when W/L ratios vary between 0.03 and 0.5. The required number of training data-points depends on the range of model as well as the complexity of structures. For example, case I requires 20 training inputs to get a prediction error less than 3% whereas the same accuracy is achieved for case II using 30 training data points [3.8]. Table 3.4 shows the properties of the neural network models and the prediction errors for these two cases. Another model is developed to predict the combined case where the aspect ratio ranges from 0.03 to 4. Figure 3.12 shows the capacitances extracted from these models. For the structures 3.11a and 3.11b, a comparison is shown in Figure 3.13 for different metal layers 1M2 and 2M2, with and without 1M1 layer grounded.

Table 3.4. Neural network parameters for modeling the capacitances

Output	Parameter	NN Structure	# of Training Inputs	Learning Rate	Prediction Error	
					RMSE	%RMSE
Case I (High W/L)		2-6-1	20	0.001	0.14	0.8
Case II (Low W/L)		2-8-1	30	0.001	0.47	2.8
Combined case		2-10-1	40	0.001	0.59	3

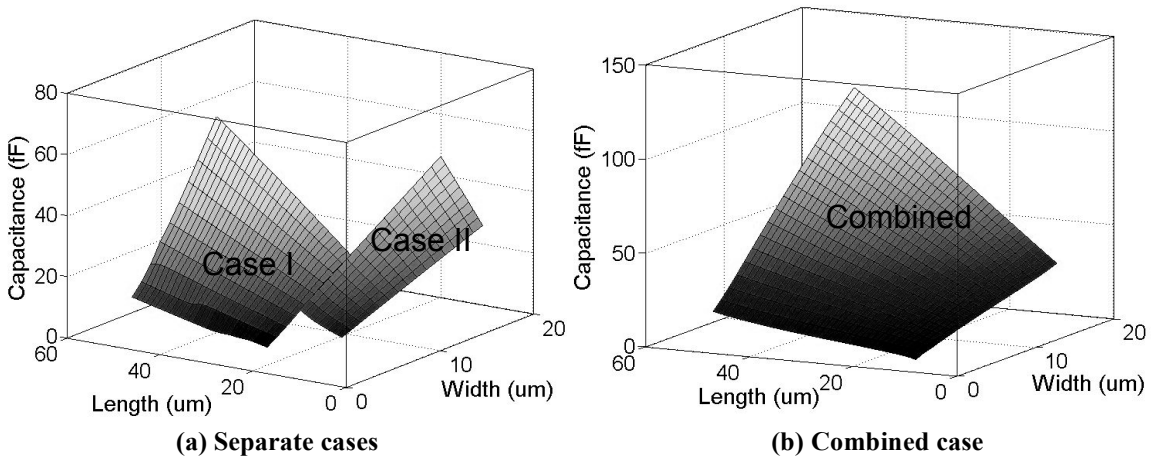
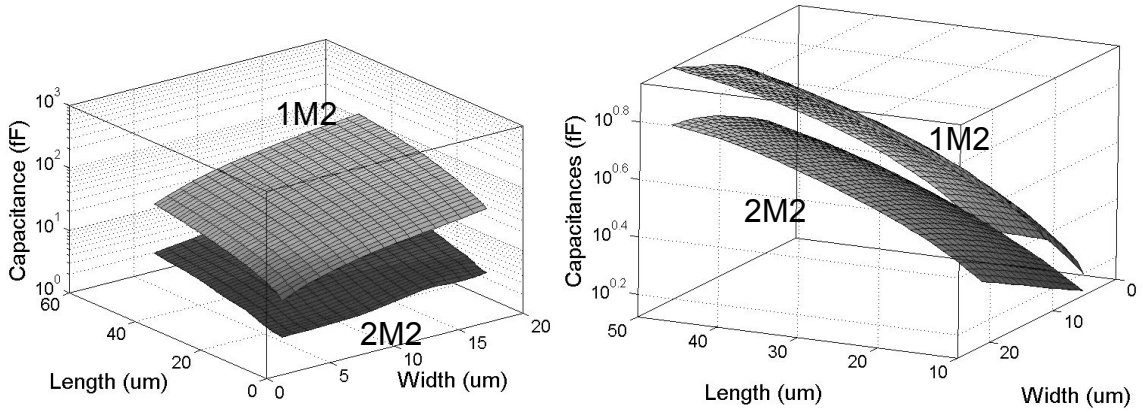


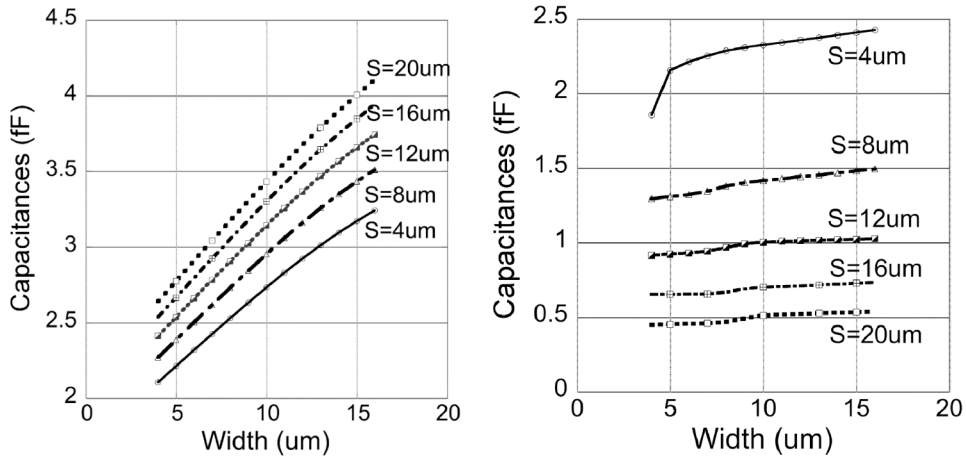
Figure 3.12. Modeled capacitances for different aspect ratio cases using the structure 3.11a for 1M2 lines over 1M1 ground.



(a) Capacitances with ground plane **(b) Capacitances without ground plane**

Figure 3.13. Modeled capacitances for lines on 1M2 and 2M2 layers with and without 1M1 ground planes.

For the cases, as shown in Figure 3.11g-3.11l, neural-network models are developed using three input parameters. For the structure shown in Figure 3.11g, the 'to-ground' self-capacitances (C_{11}) and coupling capacitances (C_{22}) with varying width and spacing for the fixed length (30μm) 2M2 layer lines are shown in Figure 3.14.



(a) **(b)**

Figure 3.14. (a) Self-capacitances; (b) coupling capacitances for the structures 3.11g (30 μm length) in 2M2 layer with 1M1 grounded.

The neural-network-based models are compared to an EM-solver and an analytic-model-based commercially available layout-extractor for randomly selected dimensions in different test layouts. The comparison results are summarized in Table 3.5. It shows

that these models can predict the capacitances more accurately than the analytical models.

Table 3.5. Comparison of capacitances using different models

Layout (Shown in Figure 3.11)	Dimensions (μm)	Capacitances (fF)		
		EM-solver	Analytic Model-based Solver	NN-based Model (This Work)
1M2 over 1M1 (3.11a)	W=4 L=11	6.27	6.05	6.13
	W=12 L=10	14.8	14.70	14.85
2M2 over 1M1 (3.11a)	W=7 L=26	3.01	2.69	2.95
	W=14 L=8	1.72	1.82	1.74
2M2 over 1M1 (3.11g)	W=11 L=13 S=31	C11=2.09	C11=1.95	C11=2.11
		C12=0.09	C12=0.11	C12=0.085
	W=8 L=28 S=16	C11=2.89	C11=2.66	C11=2.94
		C12=0.61	C12=0.60	C12=0.60
	W=16 L=14 S=5	C11=2.09	C11=2.29	C11=2.13
		C12=1.11	C12=0.82	C12=1.06

As the neural network models are based on EM solver (IE3D and HFSS) simulations, it is expected to give results, closer to EM-solver. The percentage differences of analytic solver are more in case of 2M2 over 1M1 compared to 1M2 over 1M1 test cases. That is because the analytic solver, in general, is more accurate for closer ground planes (better parallel-plate approximation) but deviates from EM-solver for the other cases. The neural network models, developed from only 30 simulation results, are found to be accurate for a large variation of input dimensions in the modeled range. The neural network simulations of 30 test structures can be done in 1ess than a minute in a 1 GB RAM windows machines in contrast to 1-4 hrs of computation in 3D EM tools, e.g., HFSS.

3.3.3 Inductance modeling and verification

3.3.3.1 Inductance modeling

The same process parameters and modeling methods are used to estimate the interconnect inductances. In most of the cases, 2M2 (a 4μm thick layer) is chosen for the inductance simulations, as thick metal lines are more inductive than thinner metal lines. Different structures are considered as shown in Figure 3.15. The variations of inductances for structures 3.15a and 3.15b in 2M2 layer are shown in Figure 3.16a, with or without 1M1 grounded. The mutual inductances between two close interconnects are also modeled using neural networks. The inductances are extracted from EM simulations using the methodology described in [3.9]. The modeled mutual inductance variation with length and spacing for 4 μm width 2M2 lines are shown in Figure3.16b.

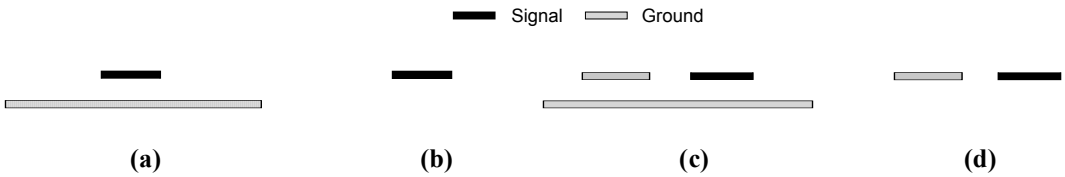
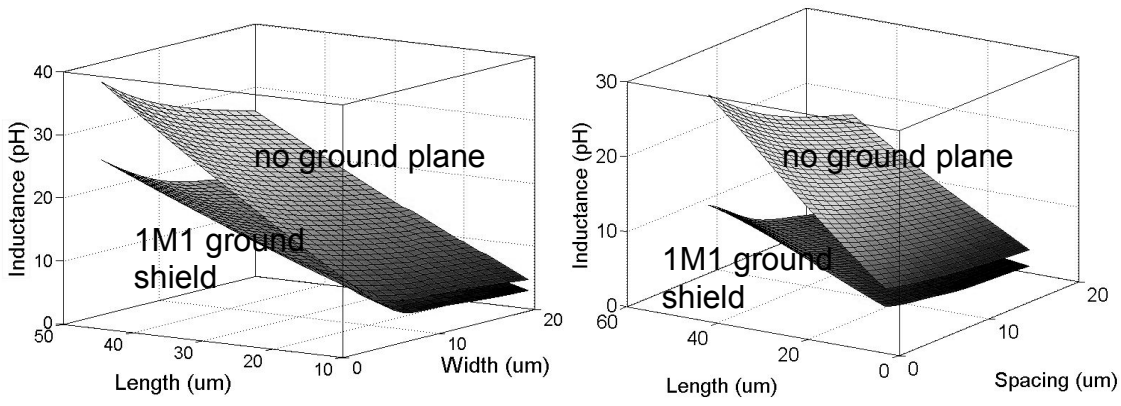


Figure 3.15. Test Structures for inductance extractions.



(a) Self-inductances **(b) Mutual Inductances**

Figure 3.16. The self and mutual inductance variation for 2M2 lines with and without 1M1 ground plane.

The values of inductances change significantly with the changes of metal layer and the layer thickness. Figure 3.17 demonstrates the differences between the inductance values for different metal layers with the same dimensions without 1M1 grounding. The strength of such a neural-network-based model lies on the fact that it can also find the dimensions for the required values of inductances. The length versus width variation for extracting same values of inductances (± 2% tolerances) for case 3.15a is shown in Figure 3.17c.

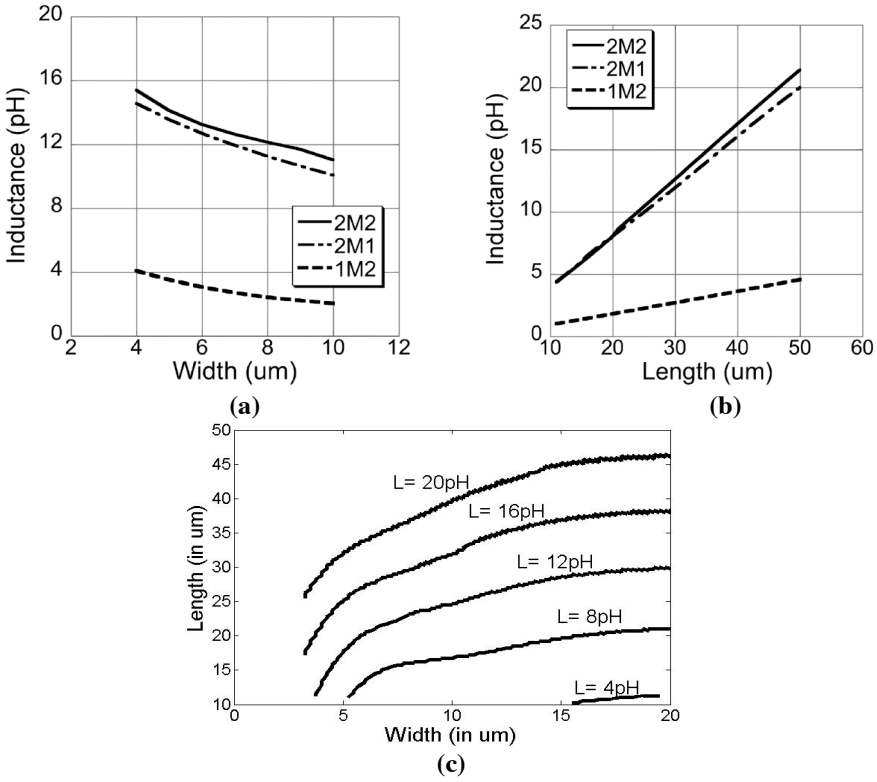


Figure 3.17. The inductance variation with 1M1 ground in different layers for (a) Length= 30µm; (b) Width =7µm; (c) the self-inductance contours for 2M2 lines on 1M1 ground.

Once trained, the neural models give a very good match with EM results for all width and length combinations in the modeled range. The models for inductances of '2M2 over 1M1' lines are extracted and compared to 3D EM-solver HFSS, a 2.5D EM tool, a semi-analytic model (provided in the design-kit), and an empirical model [2.17] in Table 3.6.

The neural network results are quite comparable to the 3D simulations in HFSS whereas the deviation with empirical models increases with changing aspect ratios.

Table 3.6. Comparison of inductances using different models

Dimensions (μm)	Inductances (pH)				
	EM-solver HFSS	EM-solver (2.5D)	Semi-Analytic Model	Empirical Model	NN-based Model
W=4 L=40	24.4	24	23.2	26	23.8
W=6 L=40	22.8	22.4	21.8	22.9	22.2
W=8 L=20	10.4	10.2	10.1	10.3	10.3
W=10 L=30	14.7	14.4	14.2	14.1	14.6
W=12 L=50	21.3	21	21.1	22	20.9
W=15 L=20	8.1	8.3	8	7.7	8.3

3.3.3.2 Comparison of commercially available tools

Commercially available tools, e.g., Assura RCX, Columbus AMS, and Calibre XL are compared to analytic model-based as well as 2.5D EM solvers. To avoid the variation with return-loop definitions, PEEC modes are preferred to return-loop inductance calculations. From PEEC modes, the signal and ground-plane inductances as well as the mutual coupling between the plates are extracted. The effective inductance is calculated using the following equation:

$$L_{effective} = L_{signal} + L_{groundplane} \pm 2K\sqrt{L_{signal} \times L_{groundplane}} \tag{3.2}$$

The sign is decided by the tool convention. For verification procedure, there are certain aspects to compare in the interconnect/transmission-line structures with ground and with/without side shielding as well as the RF lines without a definite grounds. Some of the aspects are –

1. Variation with length ($\propto$ L) and width ($\propto$ W^{-1})

2. Variation without ground plane (RF lines)
3. Variation with ground plane size
4. Changes with ground plane distance (for different layers)
5. Verification using EM tools.

The comparison results for an 80 μm long shielded line (top layer) at 1 GHz are shown in Figure 3.18 for a standard IBM SiGe-BiCMOS process. Tool X is a commercially available tool for this specific process. It is clear that the correlation is good for only a specific range of widths.

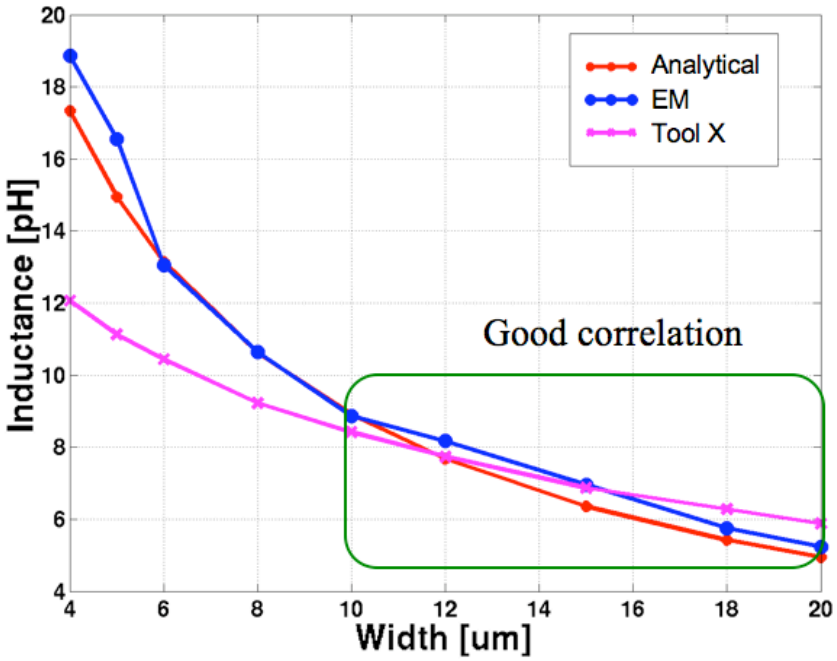


Figure 3.18. The inductance extraction correlation.

3.3.3.3 Use of meander lines in inductance model verification

As described earlier, meander lines are very compact, and they can be used to verify interconnect inductances. Also, they can be effectively used in RF/MMW circuit design as tuning inductances and if modeled properly, in matching networks as well. Two such meander line structures, fabricated in standard SiGe-BiCMOS process are shown in

Figure 3.19a and Figure 3.19b respectively. Figure 3.19c shows the EM simulation and measurement correlation between 50 and 70 GHz (targeted for 60 GHz applications) for the structure shown in Figure 3.19a.

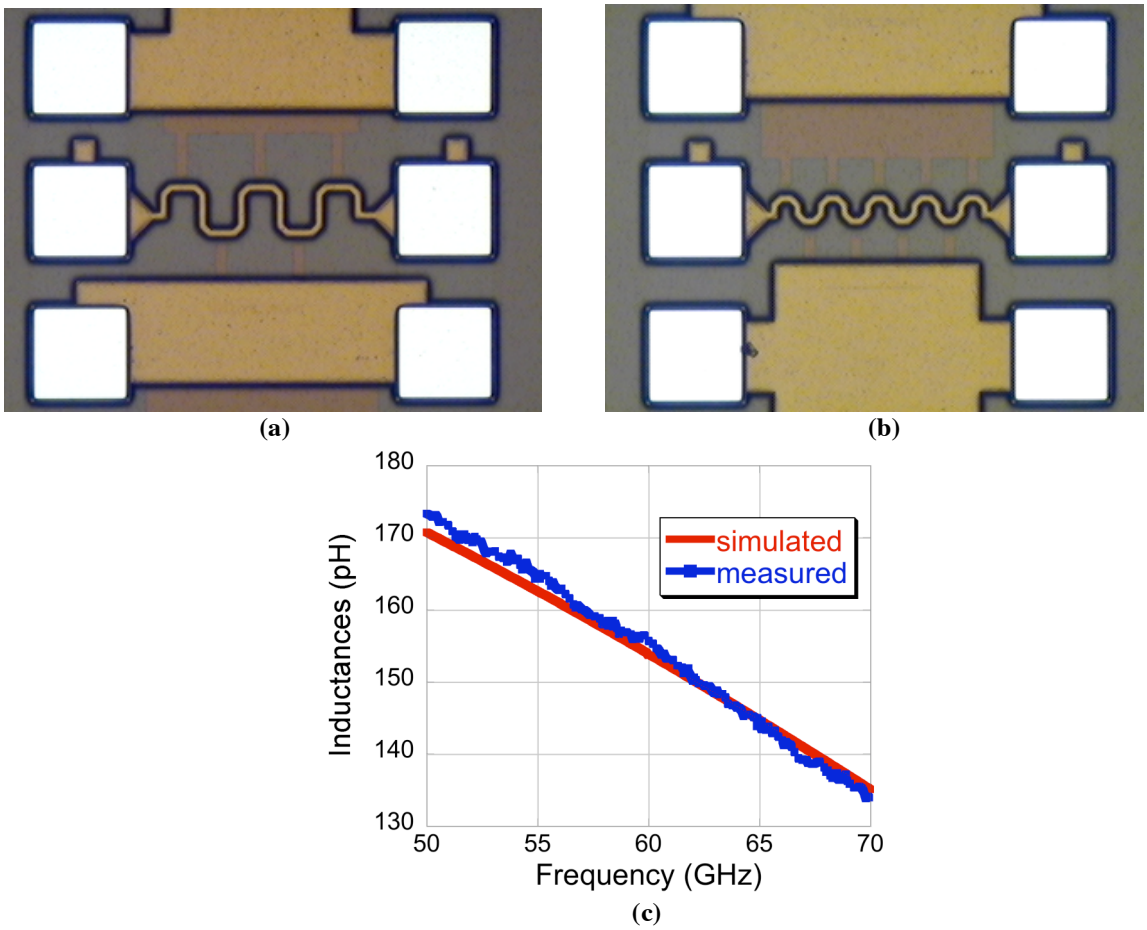
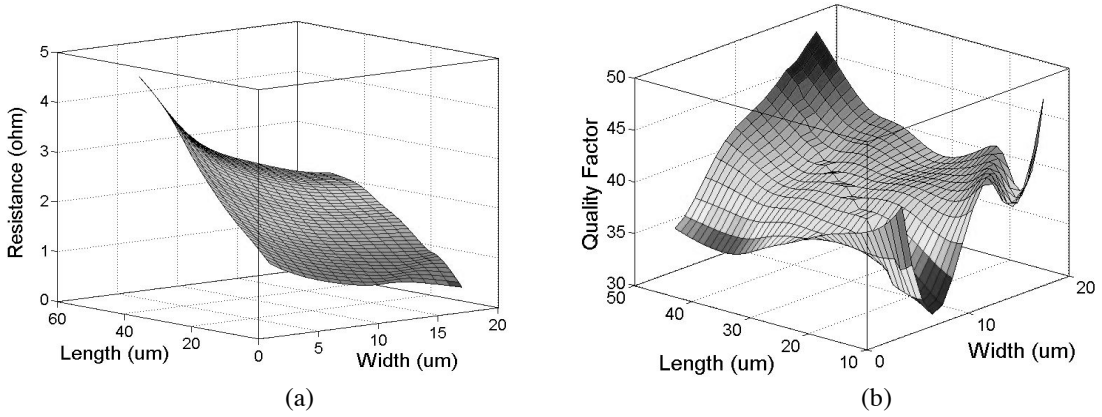


Figure 3.19. (a)-(b)Die photos and (c) measurement correlation of meander lines.

3.3.4 Resistance modeling

The interconnect (wire) resistances can be modeled using simpler models with corrections for fringing, skin, and cheesing effects. However, to develop a systematic automated parasitic extraction tool, resistances need to be modeled using neural networks as well. The modeled resistance variation of a 1M2 line is shown in Figure 3.20a. The quality factor can be extracted using models developed for the resistances and the

inductances for the same structures. The variation of quality factor is shown in Figure 3.20b for 2M2 lines over 1M1 grounds.



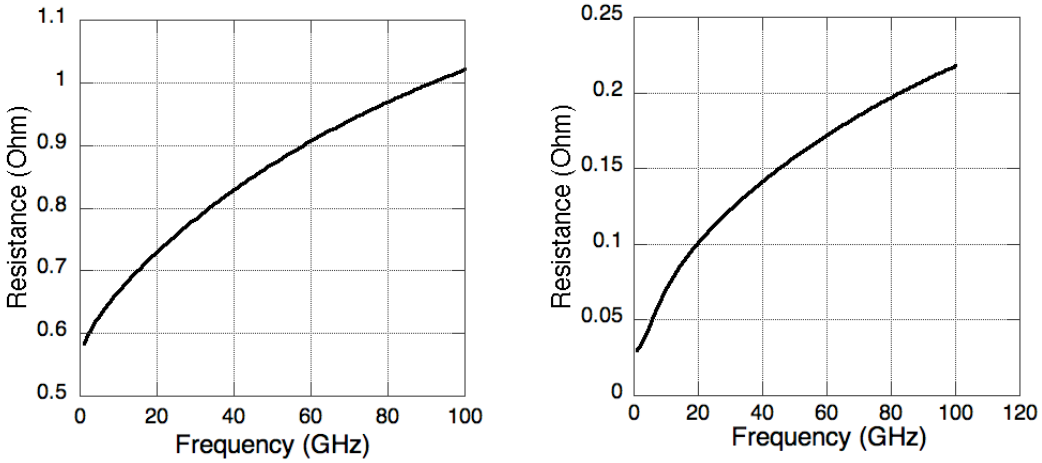
(a) (b)

Figure 3.20. (a) The variation of resistances with dimensions for 1M2 lines; (b) quality factor variation for 2M2 lines.

3.3.5 Variation with frequencies

The variations of RLC values with frequencies depend on the metal layer as well as the dimensions. Three different structures are chosen for the analysis: (a) L1= '1M2 over 1M1' line with W=2 μm and L=30 μm; (b) L2= '1M2 over 1M1' line with W=16 μm and L=30 μm; and (c) L3= '2M2 over 1M1' line with W=4 μm and L=50 μm. IE3D simulations are trusted, and a neural network approach with frequency as another input is capable of modeling the variation.

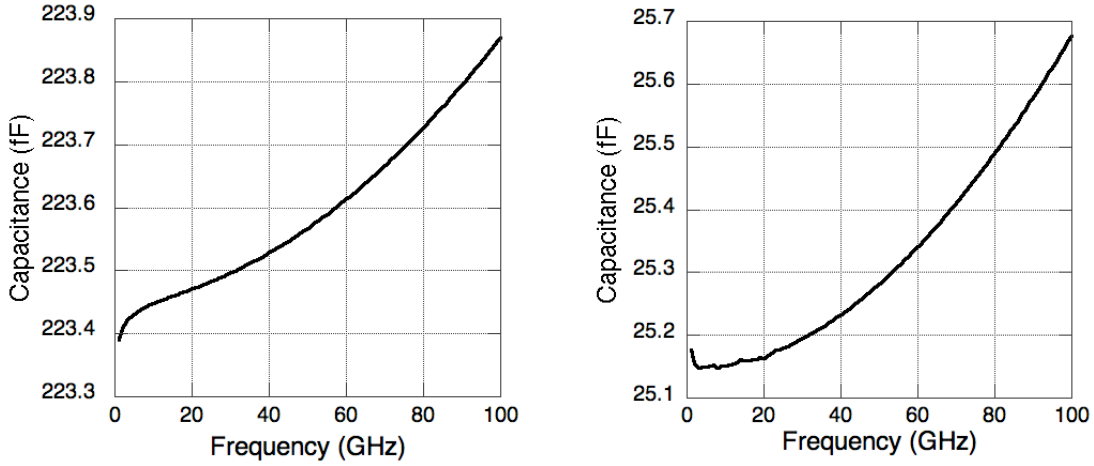
The increase of metal line resistances is mainly due to skin effect. Figure 3.21a and 3.21b show the variation of resistances for L1 and L3 respectively. The line L3 has considerably lower value for its higher thickness, and hence, the variation does not affect much in actual circuits. But M2 line resistance that changes by 100% over frequency range needs to be characterized.



(a) **(b)**

Figure 3.21. The variation of resistance with frequencies.

The capacitance variation for lines L2 and L3 are shown in Figure 3.22a and 3.22b respectively. These variation are not very significant as process variations can dominate these 0-2% changes.



(a) **(b)**

Figure 3.22. The variation of capacitance with frequencies.

The inductance variation for lines L1 and L3 are shown in Figure 3.23a and 3.23b respectively. The variations are significant, and they decrease with frequencies in both the cases.

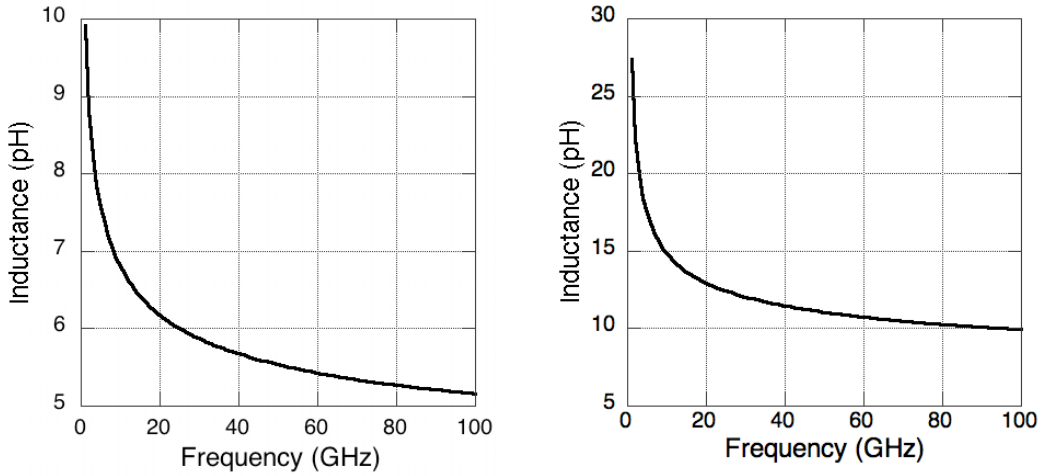


Figure 3.23. Variation of inductances with frequencies.

3.3.6 Applications

The neural network modeling technique with the automated verification procedure can significantly improve the extraction and verification time as well as the accuracy for RF/Microwave and AMS/digital applications. Since both of these methodologies are implemented using Matlab, the modeling and verification can be done in the same environment. Multi-layer perceptron models can predict the interconnect RLC networks for a range of width, length, metal layer, and frequencies. Neural models can act as alternatives to tabular or empirical models used in standard PEX tools. Also, given the design and layout constraints, the interconnect dimensions can be determined using neural models. Once trained, the neural models are 10-100 times faster than the EM solvers. In this work, the neural models are used to insert the parasitics manually in complex MMW circuits.

3.4 Parasitic benchmarking using MMW oscillators

Since, the frequency of an oscillation is the most effective comparison tool for parasitic effects rather than power or gain parameters, millimeter-wave oscillators are

used for parasitic benchmarking. Cross-coupled oscillators have been designed using models available in the ST Microelectronics design kit, and different versions of the structures are fabricated to verify the parasitic extraction and transmission line models. The schematic of the cross-coupled oscillator is shown in Figure 3.24. The varactors are not included to separate out the varactor inaccuracy from parasitic benchmarking procedure. The frequency variation is achieved by varying the dc bias conditions i.e. the source current of the cross-coupled core. Cross-coupled topology is chosen for its higher dependence on layout parasitics that can cause up to 10-25% shift in 40-50 GHz frequency ranges. The layout and die photo of one of the oscillators are shown in Figure 3.25. The average frequency of oscillation varies from 45 to 52 GHz depending on the oscillators. Source follower buffers are used to transfer the oscillation power to the 50-ohm load. One side is probed, and the other side is terminated using on-chip resistances.

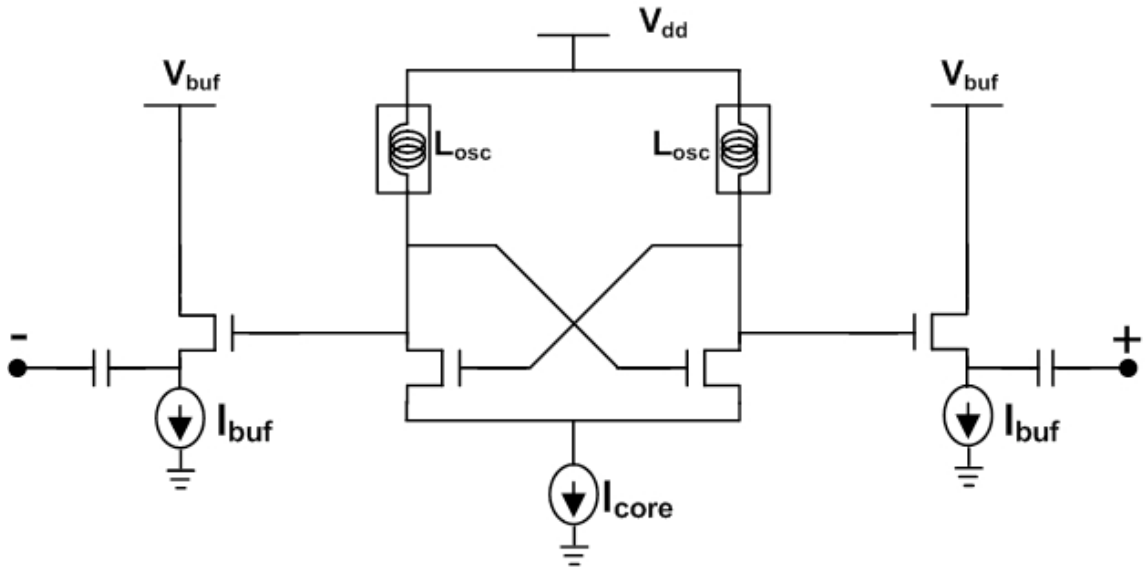


Figure 3.24. The schematic of the cross-coupled oscillator.

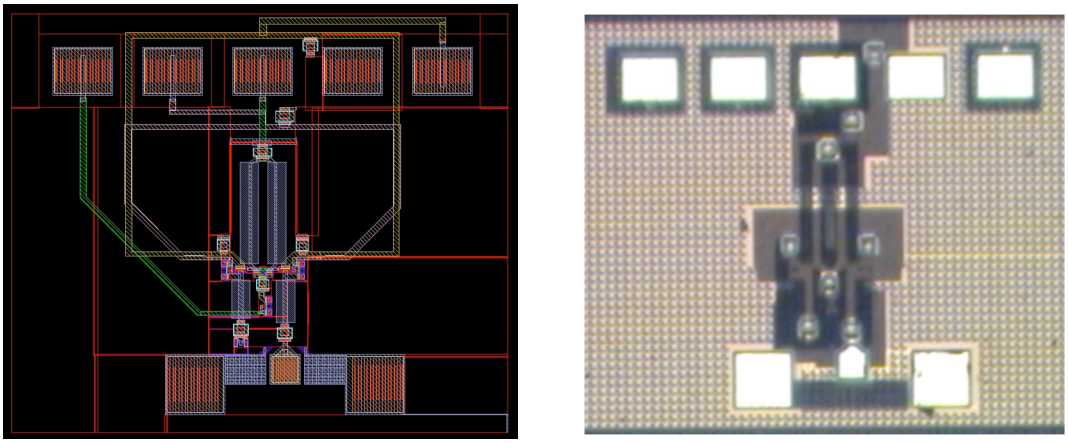


Figure 3.25. The layout and die photograph of a cross-coupled VCO.

For parasitic benchmarking, different width-length variations of the transmission line, represented by L_{OSC} are used. Total five versions of cross-coupled oscillators are fabricated. The width and length combinations used (in μm) are [200,8], [220,8], [210,6], [190,6], and [190,4]. The rest of the circuit is laid out the same way for all the structures. The parasitic-extracted schematic of the oscillators is shown in Figure 3.26.

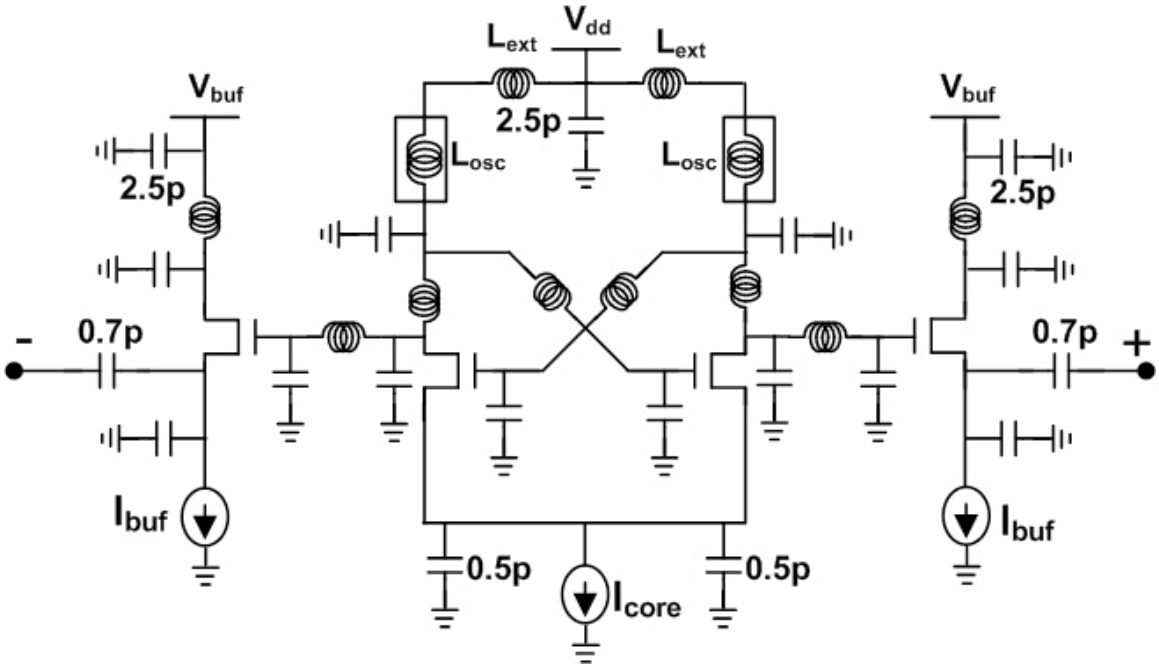


Figure 3.26. The schematic of oscillator with extracted parasitics.

Only the most sensitive components are shown in the figure. The substrate is assumed to be grounded, and in actual layout, the substrate resistance is reduced by using rings around the devices and appropriate substrate grounding. Now to account for the changes for the transmission line dimensions, the setup is shown in Figure 3.27. Inductors L_{ext} s are moved to the other side of L_{OSC} and are combined to L_t. In measurements, one-port is terminated by on-chip 50-ohm resistors. The highlighted portion remains the same for all the oscillators.

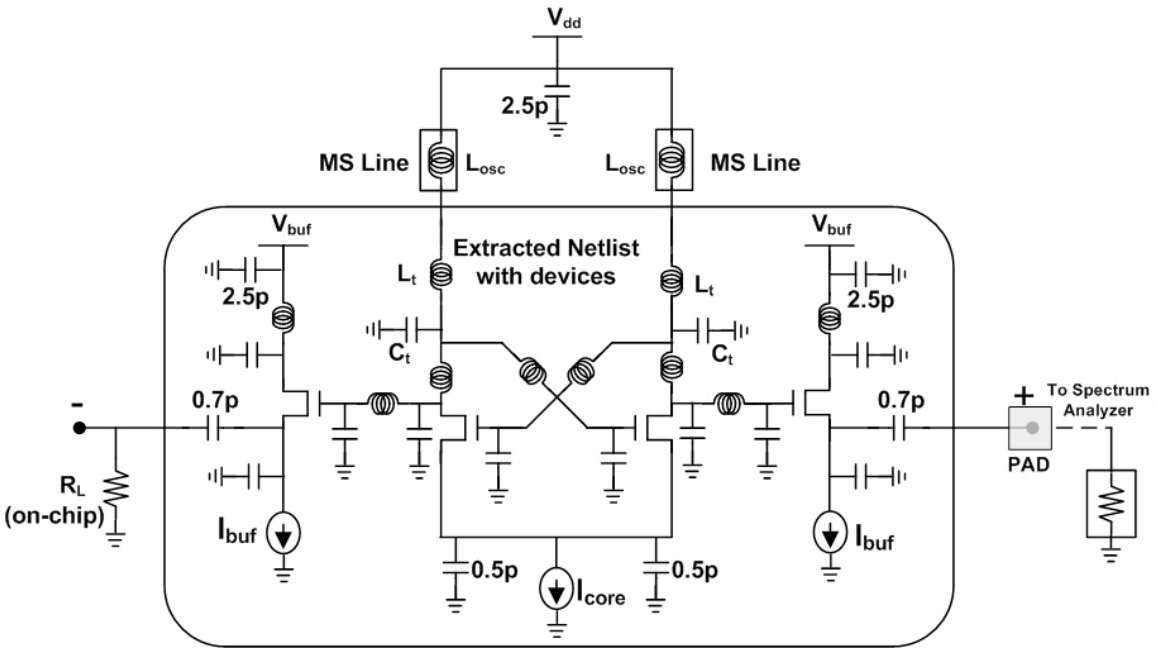


Figure 3.27. The parasitic benchmarking set up.

The transmission-line model is developed using separate test structures. The micro-strip-line structure and the model versus measurement comparisons are shown in Figure 3.28. The ground planes are slotted to satisfy the metal density requirements. The transmission line dimensions are changed to vary the oscillation frequencies, and hence, parasitic extraction is verified in a wide frequency range i.e. ~9 GHz around 50 GHz. The

center frequency is chosen to be 50 GHz targeting 60 GHz WPAN applications with IF varying from 10 to 12 GHz.

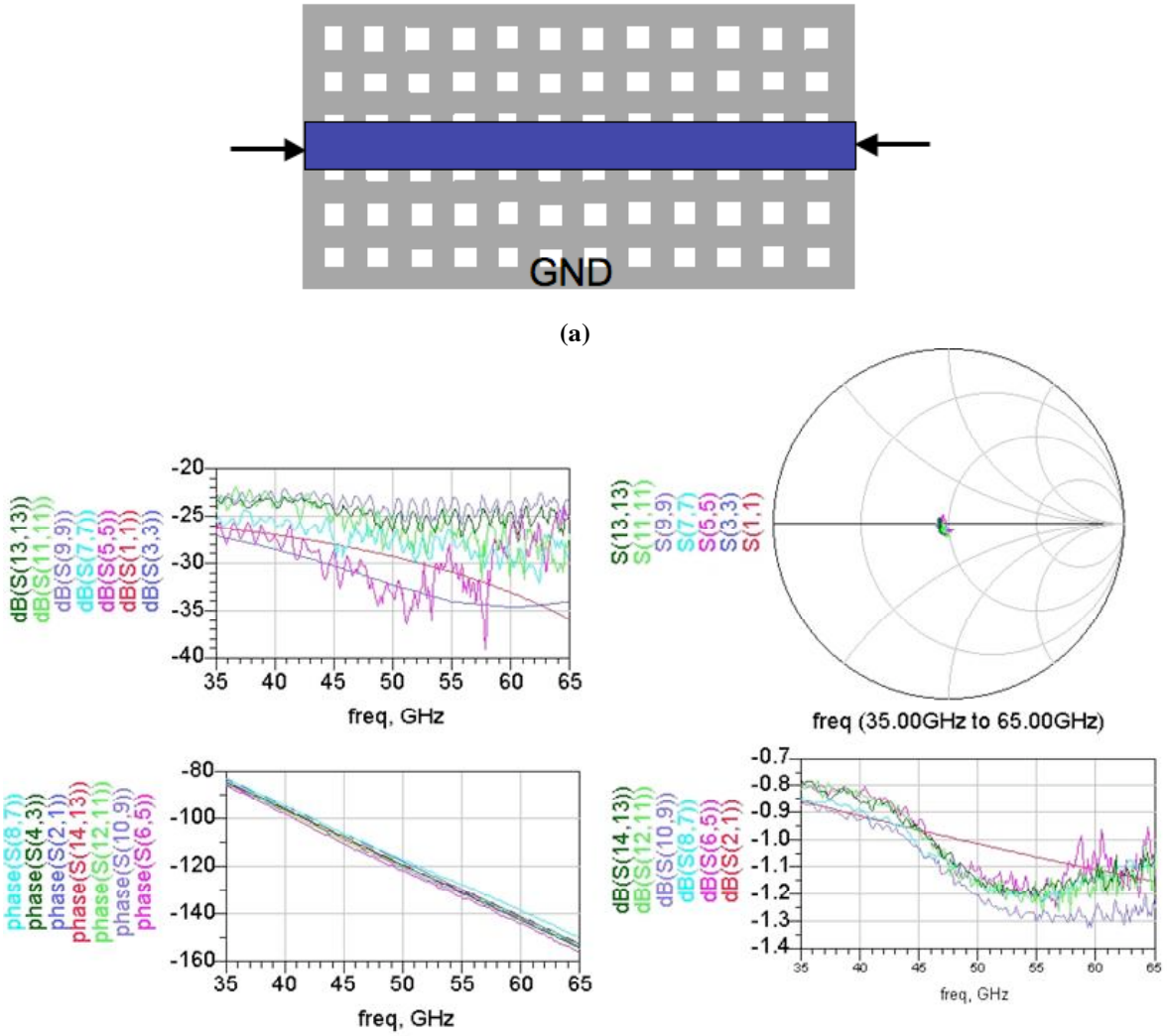


Figure 3.28. (a) Micro-strip line structure and (b) ADS setup/measurement correlation for 8 µm wide and 1 mm long line with different de-embedding approaches and multiple chip measurements.

The performance summary for different oscillators is shown in Table 3.7. The oscillator naming convention is shown in the table. Five dies are measured to evaluate the average frequency for a certain bias condition. The output (before de-embedding 6 dB loss) and phase noise plots for one of the oscillators are shown in Figure 3.29.

Table 3.7. The performance summary for the oscillators

Oscillator name	MS line dimensions	Layout name	Frequency variation (GHz)	Maximum O/P power (dBm)
CC1	[200,8]	CC1	50.6-53.5	-5
CC2	[220,8]	CC2	48.1-50.9	-3.9
CC3	[210,6]	CC3	46.4-49.3	-4.0
CC4	[190,6]	CC4	49.1-51.9	-4.6
CC5	[190,4]	CC5	45.1-47.9	-4.3
Best phase noise for all the oscillators = -95 dBc/Hz @ 1 MHz offset. Power consumption varies from 2-15 mW (for cross-coupled core) and 3-15 mW (for buffers). Hence, total power consumption = 5-30 mW for oscillations.				

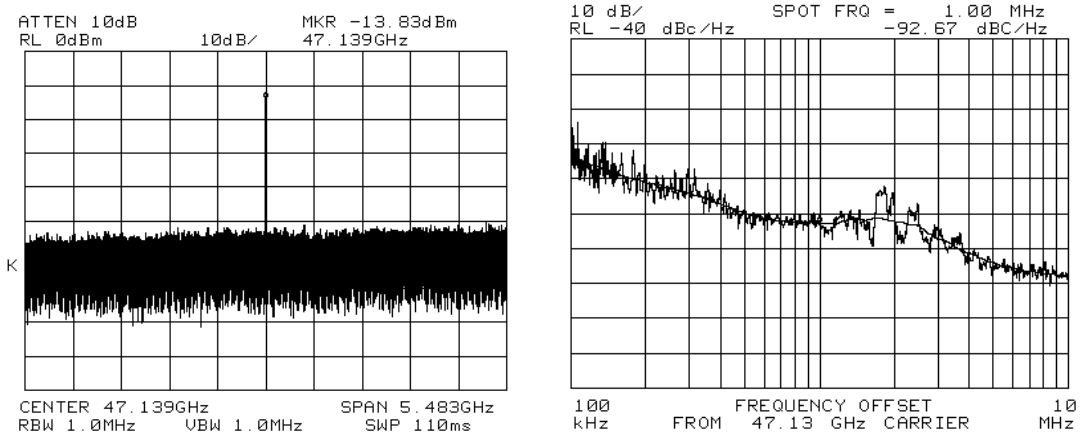


Figure 3.29. The output and phase noise plots for one of the oscillators.

The parasitic-benchmarking accuracy depends on the accuracy of the device model parameters that can affect the frequency of oscillation. That is why the verification set up is confirmed with several bias points i.e. the device model parameter variations with dc conditions. One set of frequency comparison is shown in Table 3.8.

Table 3.8. The comparison of measured and simulated performances for CC3

DC bias conditions				Meas freq (average) GHz	S. D. (meas freq) GHz	Simulated frequency (GHz)	Diff (GHz)
V_{dd} (V)	I_{core} (mA)	V_b (V)	$2I_{buf}$ (mA)				
1.2	2	1.3	4	**50.65**	0.238	50.99	0.34
1.2	5	1.3	4	**49.6625**	0.149	49.8	0.1375
1.2	8	1.3	4	**49.005**	0.067	48.93	0.075
1.5	2	1.3	4	**49.9975**	0.123	50.62	0.6225
1.5	5	1.3	4	**48.9375**	0.063	49.13	0.1925
1.5	8	1.3	4	**48.1825**	0.084	48.13	0.0525
1.2	2	1.3	8	**50.67**	0.224	51.03	0.36
1.2	5	1.3	8	**49.6825**	0.067	49.73	0.0475
1.2	8	1.3	8	**48.9075**	0.081	48.88	0.0275
1.5	2	1.3	8	**50.145**	0.126	50.7	0.555
1.5	5	1.3	8	**48.96**	0.042	49.13	0.17
1.5	8	1.3	8	**48.1425**	0.065	48.17	0.0275
1.2	2	1.6	4	**50.895**	0.187	51.15	0.255
1.2	5	1.6	4	**49.9175**	0.175	49.92	0.0025
1.2	8	1.6	4	**49.1625**	0.075	49.14	0.0225
1.5	2	1.6	4	**50.5825**	0.165	50.91	0.3275
1.5	5	1.6	4	**49.4925**	0.119	49.66	0.1675
1.5	8	1.6	4	**48.855**	0.080	48.82	0.035
1.2	2	1.6	8	**50.9125**	0.312	51.16	0.2475
1.2	5	1.6	8	**49.925**	0.126	49.89	0.035
1.2	8	1.6	8	**49.1325**	0.065	49.1	0.0325
1.5	2	1.6	8	**50.675**	0.222	50.97	0.295
1.5	5	1.6	8	**49.525**	0.189	49.64	0.115
1.5	8	1.6	8	**48.8375**	0.075	48.81	0.0275

Now the benchmarking procedure can be followed using intrinsic parasitics or extrinsic parasitics for active devices. The complexity of the multi-finger device (NMOS) connections can be reduced by validating them using measurement results. The complete verification procedure is shown in Figure 3.30, where the device model is accounted with the device parasitics as shown. The difference between measurement and simulation with parasitic components can be further reduced using the tuning components L_t and C_t. They represent the effective variation of parasitics from extracted models. The variation of CMOS model can affect the power but the parameters that are important to determine the frequency can be included in L_t and C_t for one of the oscillators, chosen for modeling/tuning.

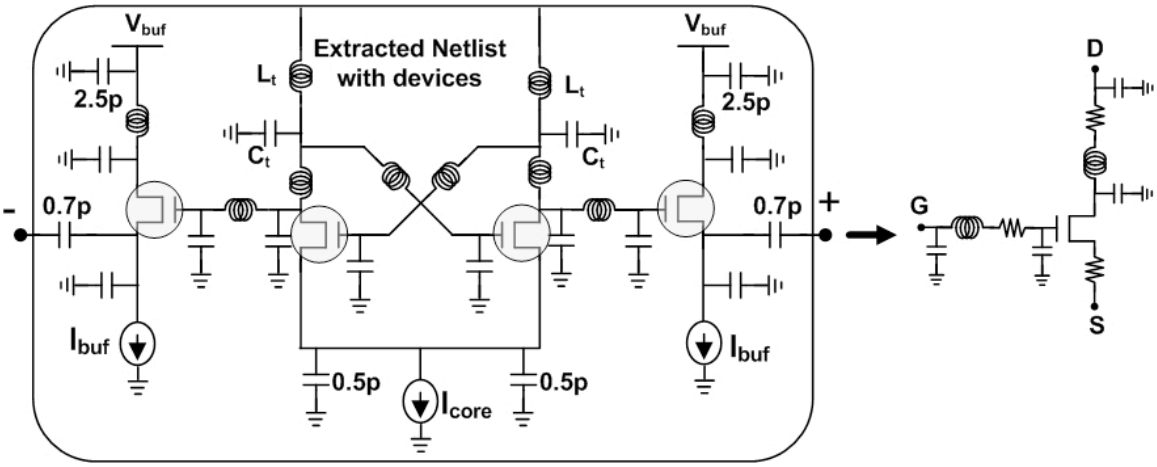


Figure 3.30. The topology based on device measurements.

The methodology is validated by choosing one nominal bias point for one of the oscillators (CC1), and, the developed model is applied to all five oscillators for 24 bias points. The effects for resistances are very small compared to inductances and capacitance except around the devices. Also the drain inductance is more significant (around 10% difference for 10 pH value) compared to the inductance between drain and gate connections (less than 3% for 10 pH value).

The measurement correlation with varying bias conditions for different oscillators is represented in Figure 3.31. It is observed that the correlation is better than 1% for most of the oscillators. The variation in CC5 is more than others as the model is based on CC1 (farthest in frequency from CC5). The variation for oscillator CC5 can be explained by the different width of the transmission line (4 μm whereas the validated micro-strip line width is 8 μm), variation of parasitic components with frequencies, and different oscillation frequency ranges that require different tuning values for [L_t, C_t]. The average modulus percentage variations are shown in Figure 3.32.

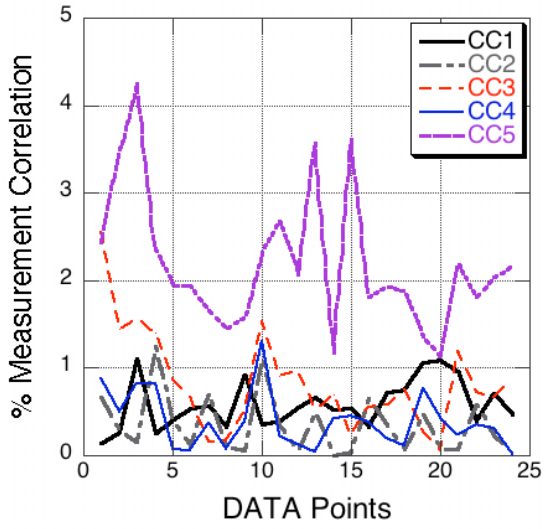


Figure 3.31. The measurement correlation for different oscillators.

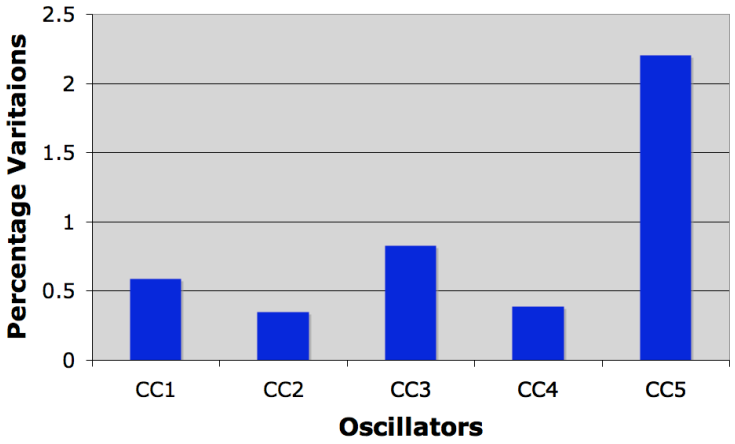


Figure 3.32. The average error for the oscillators.

3.5 Summary

In this chapter, state-of-the-art silicon-based multilayer RF process parameters are utilized to extract the resistive, capacitive, and inductive components of the layout interconnects. Neural network models are developed using EM simulation results from a given set of passive interconnect structures. Additionally, an automated layout generation methodology is developed using MATLAB codes/Perl scripts, and it is used for verification of the parasitic extraction methodologies. The proposed verification approach is demonstrated using automatically generated passive test structures and ring oscillators. The set of interconnect structures used exposes majority of layout scenarios. EM extractions and neural-network-based modeling strategies are adopted to predict the capacitances as well as the inductances for different test structures with varying dimensions in a defined layout environment. The developed models can estimate the capacitive and the inductive effects accurately (1-3% prediction error depending on the complexity of structures as well as the training data size). The variations of the RLC components are determined using different test structures. Finally, a parasitic benchmarking procedure is developed using cross-coupled oscillators in a state-of-the-art 90 nm CMOS process.

Chapter 4

Parasitic Effects in MMW Circuits

4.1 Introduction

Millimeter-wave has been a medium for automotive, sensor, and defense applications for a long time. For military and defense applications, they use 77 GHz, 94 GHz or even higher carrier frequencies. But, license-free frequency bands are essential for any viable commercial applications. The bandwidth of the frequency band should also be large enough to be able to support multi-gigabit transmission over 1 m - 10 m distance. The worldwide license-free 59-64 GHz band is the most suitable one (59-66 GHz in Japan and Europe, 57-64 GHz in USA) [1.2] to provide enough bandwidth to reach multi-gigabit throughput using very simple modulation schemes, e.g., amplitude shift-keying (ASK) or binary phase shift-keying (BPSK). More complex schemes, e.g., quadrature phase shift-keying (QPSK) or orthogonal frequency-division multiplexing (OFDM) can result in a higher than 10 Gbps data rate. The challenges include a significant attenuation of the wireless channel at 60 GHz [1.5], silicon-based low-cost high performance implementation of the front-end circuits, parasitically-optimized transceiver block design, output power of the transmitter, noise figure and sensitivity of the receiver, low-cost effective package, and compact high-gain antenna implementation. Since, initially targeted low cost implementation demands best/optimum performance from CMOS processes for different blocks; a parasitically optimized design is a must. In this chapter,

60 GHz transceiver blocks are considered to demonstrate the effects of interconnect parasitic components. Circuits are designed in SiGe-BiCMOS and CMOS technologies to demonstrate the potential of silicon-based transceiver design at 60 GHz or higher frequencies. For the same feature size, SiGe HBT provides higher gain and power handling capability but CMOS circuit have their advantages in terms of cost and baseband-integration. Hence both the technologies are used to demonstrate the effects of parasitics in MMW circuits.

4.2 Transceiver system architectures and sensitive blocks

The receiver blocks for two different architectures are shown in Figure 4.1. In the direct-conversion architectures, the tuning of the VCO is very important, and the mixer design is very critical since it direct converts the RF signal to base-band. On the other hand, super-heterodyne architecture has more blocks though the tuning requirements are less stringent in the VCO#1 or the LO. The VCO#2 that operates below 10 GHz is less dominated by parasitics, and hence, it is easier to design this VCO to fulfill base-band requirements.

In some super-heterodyne architectures, a separate IF VCO (VCO #2) can be eliminated by using frequency dividers from the LO. One such frequency planning would be to use 48.4 GHz as LO frequency and to generate 12.1 GHz IF oscillations through divide-by-4 block.

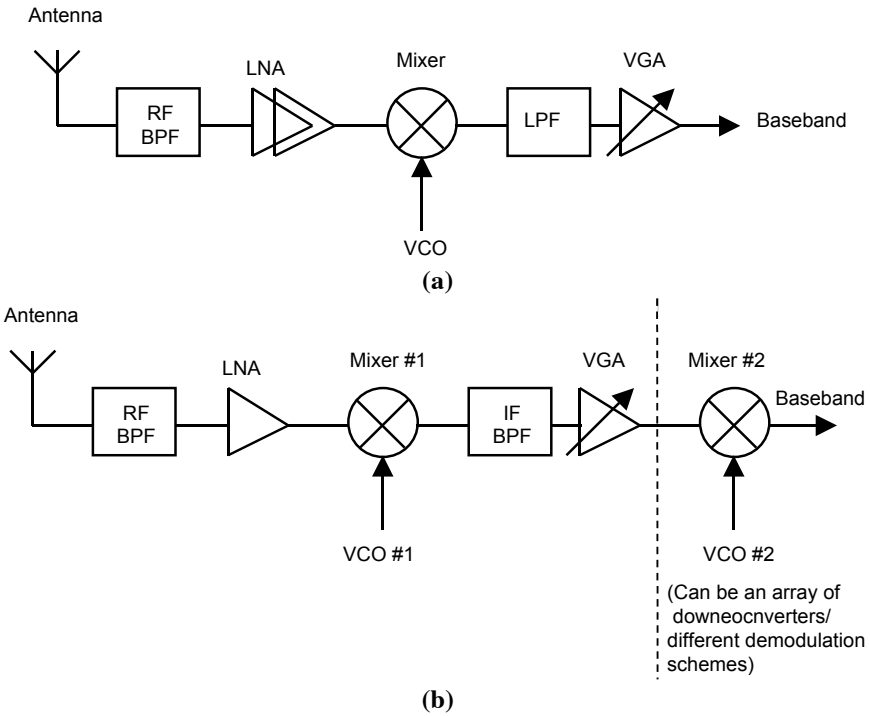


Figure 4.1. Receiver using (a) direct-conversion architecture; (b) super-heterodyne architecture.

The low noise amplifier (LNA) and mixer blocks are usually transmission-line dominated designs, and they can be characterized by measurements from transistors and transmission-line test structures. But there are variations depending on the topology. Whereas a single gate mixer [4.1] design in CMOS process is mostly transmission-line-based, a double Gilbert-cell mixer [4.2] design demands an accurate characterization of parastics. However, in the design of IF or baseband variable gain amplifiers (VGAs), the parasitic effects may not be that prominent but they need to be included for better performance characterization.

A super-heterodyne transmitter architecture is shown in Figure 4.2. There are some common blocks with receiver but the requirements are different. Also power-amplifier (PA) block is usually realized using big transistors, and hence, the modeling of parasitics around the devices becomes important to get a good input, output and inter-stage

matching. A frequency planning is shown in Figure 4.2 for 60 GHz applications. Two VCOs are tuned at 52 GHz and 8.5 GHz respectively. The PA output is tuned at 60.5 GHz to cover 57-64 GHz band.

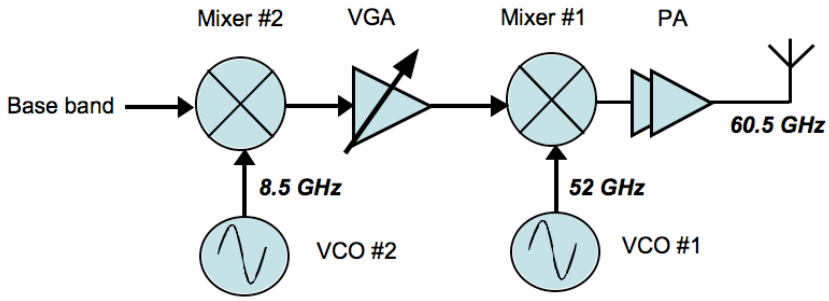


Figure 4.2. A super-heterodyne transmitter architecture.

For a complete transceiver system, other than the design of different blocks, the co-design of the blocks and the layout connections between blocks as well as to external pads become critical. The layout optimization challenges for an integrated system will be described in the following chapter.

For any architecture, there are some common RF blocks like VCO, PLL, LNA and PA. The performance requirements change depending on the implementations. For example, in amplitude-shift-keying (ASK) modulation schemes, the linearity of PA is not that important but for QAM modulation topology, it becomes an important performance parameter. As far as the design methodology is concerned, amplifiers mainly consist of device blocks and matching networks. Matching networks, being implemented using already characterized transmission lines for a mature process, can be accurately realized considering only the active device parasitics. So, for LNA or PA, only parasitics around active devices (single or cascode-connected) need to be accounted while evaluating the matching conditions. But the circuits more prone/sensitive to parasitics are VCOs and frequency dividers that are essential components of the integrated frequency synthesizer.

Also, the role of parasitics varies with different topologies of oscillator. In this work, circuit layouts are differentiated into two types depending on parasitic sensitivities. Type 1 layouts are identified with multiple connections to active devices and the parasitic effects in the order of 10-40%. Type 2 layouts are mostly transmission-line dominated with interconnect effects in the range 1-10%. Different layout topologies are presented in Figure 4.3 and Figure 4.4 respectively.

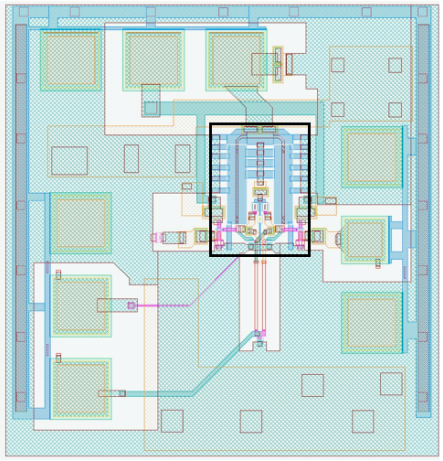


Figure 4.3. A 'type 1' layout.

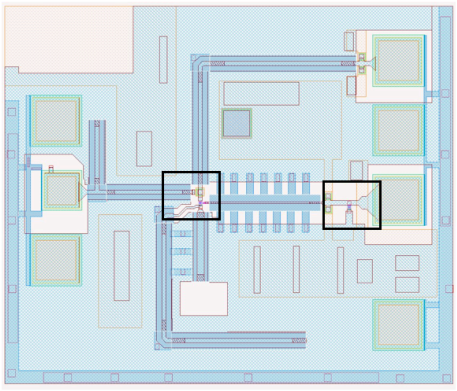


Figure 4.4. A 'type 2' layout.

Figure 4.3 shows the layout of a SiGe cross-coupled oscillator (type 1), where there are substantial effects of parasitic inductances and capacitances. In Figure 4.4, the layout of a negative-resistance SiGe oscillator is shown. It is a type 2 transmission-line-dominated layout and hence, less sensitive to interconnect parasitics.

The design and layout optimization flow is shown in Figure 4.5. In the following sections, the estimation and optimization of parasitics are demonstrated for active devices and different circuit blocks. In the next chapter, the co-design of different blocks and the complete system design issues will be discussed.

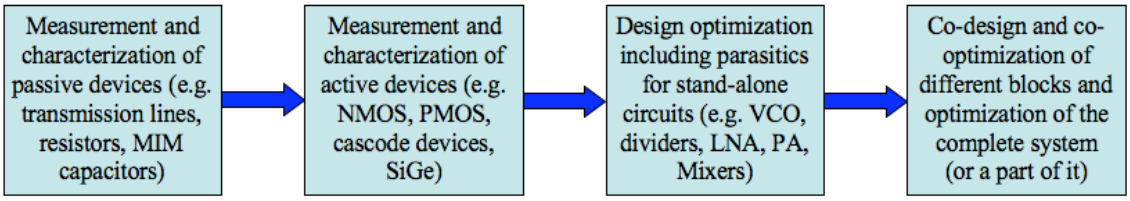


Figure 4.5. The design and layout optimization flow.

4.3 Active device related issues and examples

The extraction and minimization of the layout parasitics have become very important for the aggressively scaled devices with reduced device capacitances, and as a result, the performance is limited by the device structures and the layout constraints. For the applications above 30 GHz, capacitances and inductances dominate the active device response, and hence, the modeling and extraction of device parasitics have become extremely critical. For small devices, the device-capacitance to parasitic-capacitance ratio, and for large devices, multi-finger layout configurations demand an accurate estimation of parasitics in active device models.

4.3.1 Effects of parasitics on SiGe HBT devices

To study the small signal behavior of a hetero-junction bipolar transistor (HBT), a Gummelpoon-based model is proposed. The transistor, chosen for intrinsic model extraction, is a state-of-the-art SiGe HBT with an emitter length of 10 μm and an emitter width of 0.12 μm. The intrinsic model is shown in Figure 4.6a. A novel feature of this model is the inclusion of a capacitance (C_{bi}) in parallel with the base resistance R_{bi} [1.7].

These parameters are required to accurately model the raised extrinsic base structure used in advanced SiGe-BiCMOS processes. Here, the intrinsic interconnect resistances are denoted as R_{bi}, R_{ci} and R_{ei}. The values of R_{bi}, R_{ci}, R_{ei} are determined by plotting [Figure 4.6b] the real parts of $(Z_{11} - Z_{21})$, $(Z_{22} - Z_{21})$ and Z_{12} versus $1/I_B$ from the open-collector Z-parameters after de-embedding, where I_B is driven base current with zero collector current. The inductive effects can be estimated from the imaginary parts, but for a single finger device, the resistive effects are more pronounced below 50 GHz. A robust de-embedding procedure [4.3] is used to model the pad parasitics. The intrinsic device model is accurate over a wide frequency range as shown in Figure 4.7.

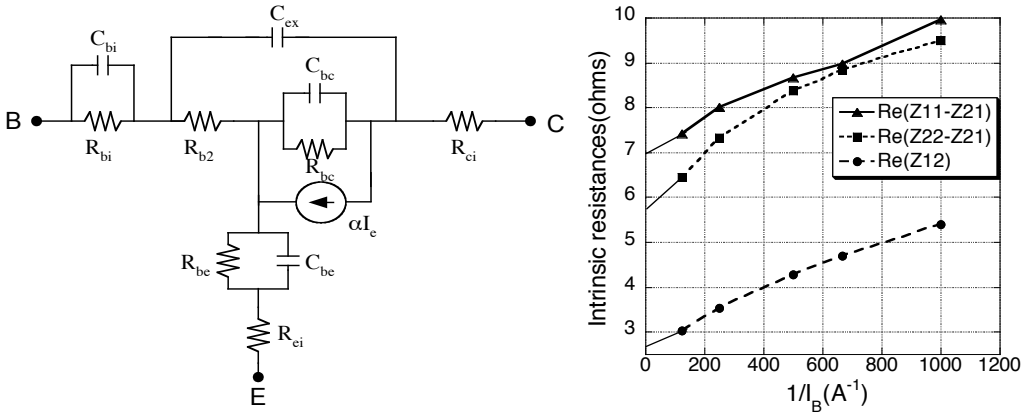


Figure 4.6. (a) The broadband small signal model for SiGe HBT; (b) the extraction of intrinsic resistances.

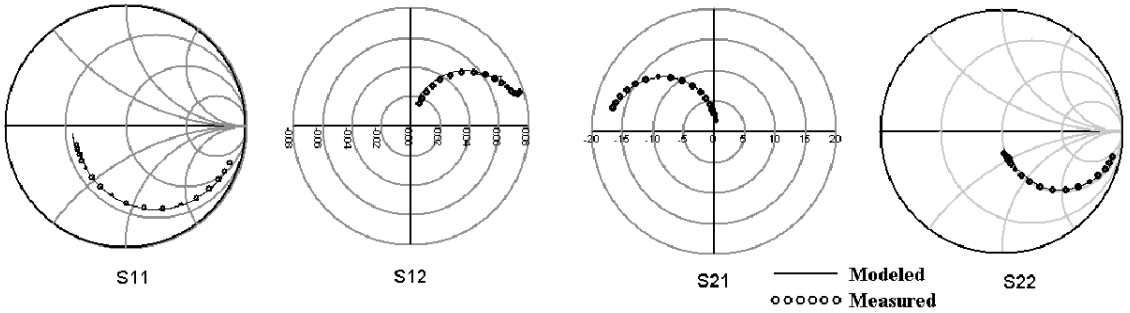


Figure 4.7. The measured and modeled intrinsic S-parameters after de-embedding (2 to 80 GHz, V_{ce}=0.8V, I_B=25 μA for a 10 x 0.12 μm^2 device).

Using the same model, the effects of possible parasitics are studied, adding extra components. The possible parasitics are identified as –

(i) Distributed capacitances from the base (C_{bg}), collector (C_{cg}) and emitter (C_{eg}) to ground.

(ii) Base-to-collector (C_{bc}) and base-to-emitter (C_{be}) coupling capacitances.

(iii) The inductive effects represented as L_{bi}, L_{ci} and L_{ei} respectively

(iv) The resistive effects represented as DR_{bi}, DR_{ci} and DR_{ei} respectively

Considering the reduced size of base, the C_{bg}, C_{bc}, C_{be} values are not very significant but base resistance and inductances cannot be neglected. For small signal operations, f_T and S_{21} under same load conditions represent the circuit behavior. The effects of the parasitics on these performance parameters are shown in Figures 4.8 and 4.9 respectively.

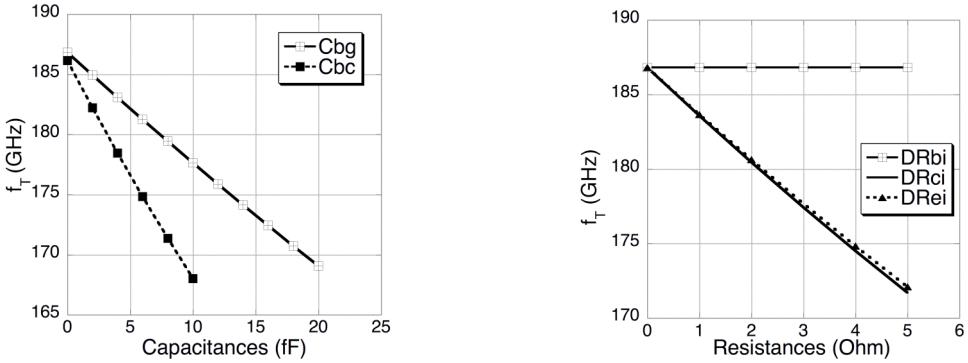


Figure 4.8. Effects of parasitics on the f_T of the SiGe HBT device.

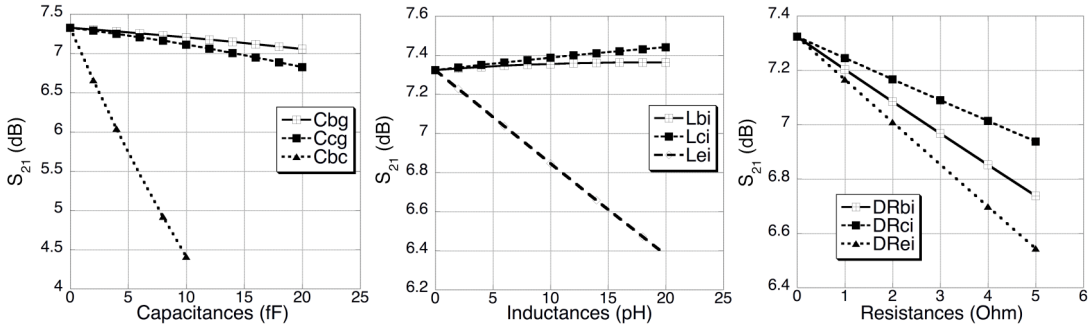


Figure 4.9. The effects of parasitics on the forward gain at 60GHz under the same matching conditions.

From Figure 4.8, it is clear that the effects of capacitances and resistances on f_T are more pronounced than the series inductances. The parasitics can also modify the forward gain parameters (at 60 GHz) as shown in Figure 4.9. Hence, they should be considered while matching the devices for amplifiers or mixers. Also, the output impedances of the SiGe devices are very critical for circuit designs. The parasitic sensitivities of real and imaginary parts of Z_{22} in common-emitter configuration (without any matching networks) are demonstrated as shown in Figure 4.10. It is evident that all parasitics are not important for the analysis of device performance in a certain configuration. These analyses would help the circuit designer to identify the sensitivity of different nodes to different parasitics, and accordingly, would help to find the proper layout methodology.

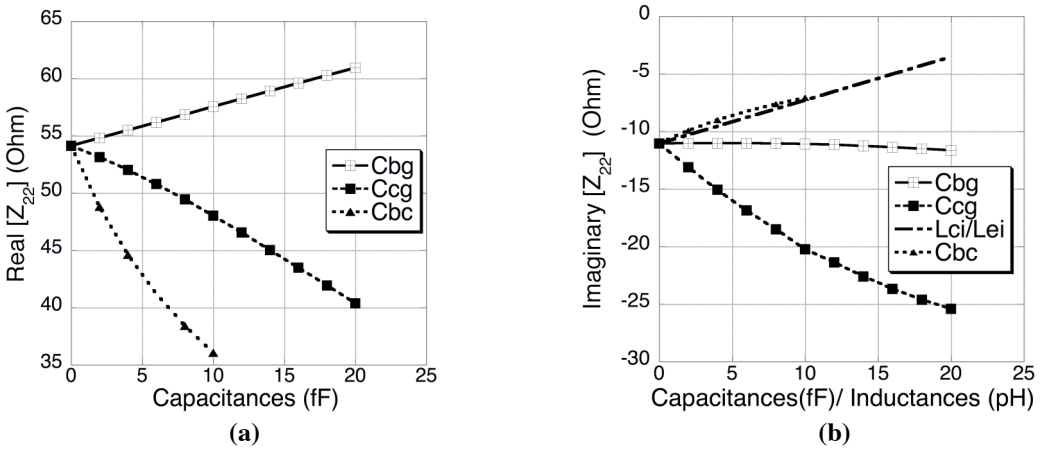


Figure 4.10. The effects of parasitics on the output impedance.

4.3.2 Identification of significant parasitics in CMOS devices

Historically, monolithic microwave integrated circuits (MMICs) have been designed using III-V semiconductor technologies that have superior performances compared to CMOS because of higher electron mobility, higher breakdown and high-Q passives. With the advent of SiGe technologies, Si-based MMW systems are made possible. However, a CMOS implementation promises lower cost and high throughput integrated solution than

its counterparts. A CMOS realization is usually aimed for comercial applications. Recently, wireless systems operating at frequencies higher than 30 GHz have been implemented with improved device layouts and process parameters [4.4,4.5]. Front-end circuits in 90/130 nm CMOS technologies have been demonstrated [4.5] with achieved f_{max} above 100 GHz. Though CMOS process suffers from low substrate resistivity and high sheet-resistance poly-silicon gates, the use of multiple fingers can significantly improve the f_T and f_{max} values. At these frequencies, accurate extraction of all the parasitics around the CMOS devices is very important. Also, the substrate effects have to be considered accurately. The structure of an NMOS device is shown in Figure 4.11.

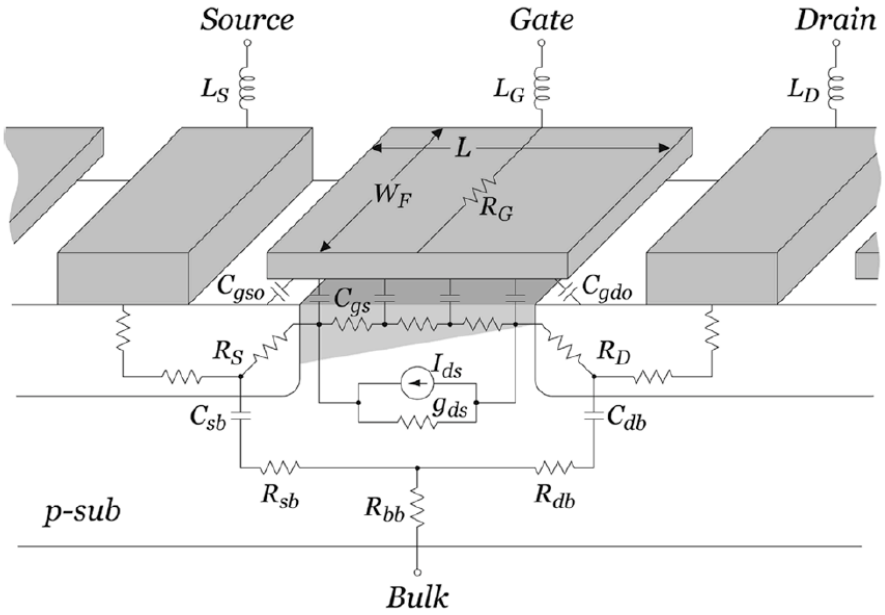


Figure 4.11. The NMOS structure with model parameters/ parasitic components [courtesy: 4.4].

The gate interconnect resistance (generally consists of salicide and poly-silicon resistances) is given by:

$$R_g = \kappa . \frac{1}{3} . \frac{W_f}{N_f L_f} . R_{g-sh} \tag{4.1}$$

κ denotes the connection factor to account for the gate contact methodology (unity for one side, 1/4 for two-sided contacts). W_f is the width of the finger. N_f is the length of the finger, and L_f is the number of fingers respectively. $R_{g\text{-}sh}$ is the gate sheet resistance. The factor 1/3 is to account for the distributed nature of RC lines across the channel (MOS transistors are usually very wide). Now, to account for the effects of the gate capacitances C_{gg} and the delay τ in small signal behavior of MOS transistors, consider the expressions for y_{21}, y_{11} of a simplified MOS model [4.6]:

$$y_{11} \cong \frac{j\omega C_{gg}}{1 + j\omega R_g C_{gg}} \tag{4.2}$$

$$y_{21} \cong \frac{g_m - j\omega(C_m + C_{gd})}{1 + j\omega R_g C_{gg}} \tag{4.3}$$

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} \tag{4.4}$$

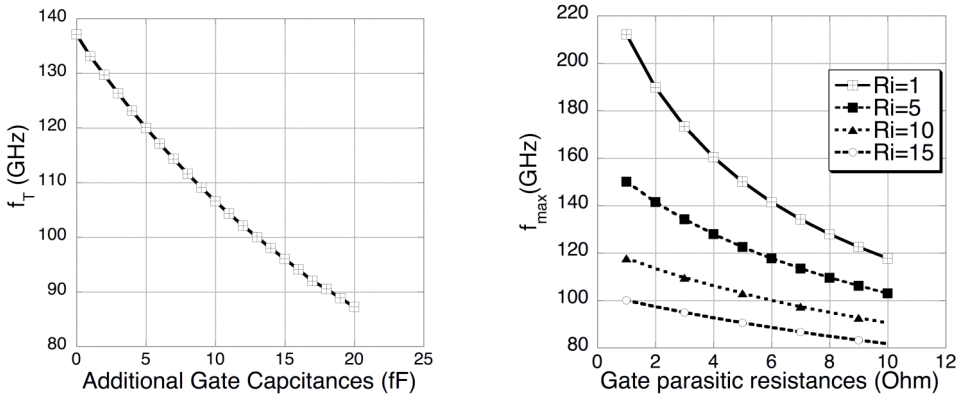
$$C_m = g_m.\tau \tag{4.5}$$

$$h_{21} = \frac{y_{21}}{y_{11}} \tag{4.6}$$

Where, C_m is the trans-capacitance derived from the delay τ and conductance g_m. The default values of the above parameters are assumed from a state-of-the-art 130 nm process. The variation of f_T (derived from h_{21}) is shown in Figure 4.12a(for g_m= 30 mS and C_{gg} without additive parasitics = 35 fF). The performance of the circuits also relies upon the value of f_{max}. From the expressions (4.2-4.6), f_T is considered to be (approximately) independent of R_g. Now, the correlation between f_{max} and f_T as a function of gate resistance after simplifications [4.7] is given by:

$$f_{\max} = \tfrac{1}{2}.f_T.\left[\frac{R_i+R_g+R_s}{R_{ds}} + \pi.f_T.C_{gd}.(R_i + 2R_g + 2.\pi.f_T.L_s)\right]^{-\frac{1}{2}} \quad \Rightarrow \quad f_{\max} = \sqrt{\frac{f_T}{2\pi R_g C_{gd}}} \tag{4.7}$$

From this expression, it can be observed that not only gate parasitics, but, the coupling capacitances, and source parasitics can also affect the f_{max} significantly. The variation of f_{max} with R_g for different R_is is shown in Figure 4.12b. f_T is assumed constant at 120 GHz. The device performance can be improved by tuning out the device capacitances with interconnect inductances and hence, increasing the f_{max}, the limit for circuit operating frequency.



(a) **(b)**

Figure 4.12. The parasitic effects in CMOS devices.

For high-speed digital applications, the signal integrity problems comes into picture, and the interconnect RC delays limit the circuit performances as the clock speed is reaching above 2 GHz. The gate-to-source capacitances degrade the performances significantly for aggressively scaled MOSFETs in 45, 65, 90 nm processes and the modeling of those parasitics should be performed accurately [4.8]. The extraction methodologies demand test-sites to model the poly-silicon to active interactions and the self-capacitances of poly-silicon as well as active diffusion (RX) layers [4.9]. The automated layout generation techniques can be very effective in modeling delays [3.2]. The substrate coupling effects are also important in RF CMOS processes. Properly grounded structures and more substrate contacts may reduce the substrate resistances but

for better device operations, it may be a better idea not to ground substrate around the devices if noise mitigation is not that important issue.

To demonstrate the characterization of interconnect parasitics around devices in sub-100 nm CMOS processes, a 40-μm-width NMOS with 40 fingers is studied in 90 nm CMOS process. The schematic with parasitics is shown in Figure 4.13a. The parasitics are estimated and included to match the measurement results. The measurement correlations with and without parasitics are shown in Figure 4.13b-d. Ports 1, 2 correspond to the measured results. Ports 3, 4 represent the device without interconnect parasitics, and port 5,6 correspond to the simulation with estimated parasitics.

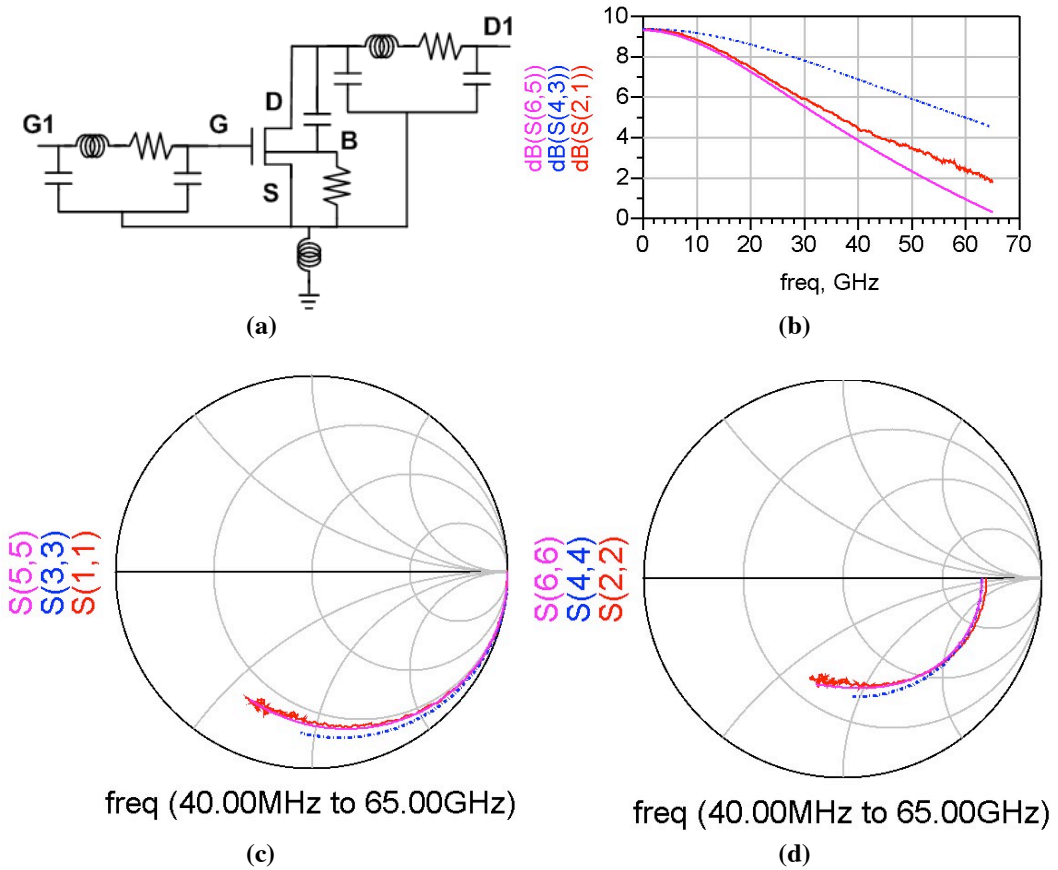


Figure 4.13. (a) The schematic, (b) gain parameters, (c) input matching and (d) output matching measurement correlation for a 40x 1 μm NMOS device with parasitics.

4.4 Parasitic estimation of sensitive blocks

In this section, the effects of parasitics on the sensitive transceiver blocks will be discussed. Several fixed-frequency oscillators and VCOs are designed, laid out and measured to demonstrate the effects of layout parasitics in CMOS and HBT technologies for a very wide frequency ranges. The shifts in center frequencies for oscillators are explained using neural-network-based models of parasitic components, and the sensitive nodes are identified to optimize the parasitic effects for a better design centering aspect. Frequency divider is identified as another sensitive block of an integrated frequency synthesizer used in a MMW transceiver. Parasitic effects in two different types of frequency dividers are studied. Measurement results are presented to support the sensitivity towards layout parasitics for different 'type 1' and 'type 2' circuit layouts. In this section, mostly resonant circuits with a compact core and pad-dominated layouts are considered. However, some examples are described in the case of MMW amplifiers where on-chip or off-chip parasitic component may affect significantly.

4.4.1 Fixed frequency oscillator examples

Fixed frequency oscillators (FFOs) are designed aiming at 60-GHz-ASK direct-conversion transmitter architecture in silicon-based processes. The ASK architecture is shown in Figure 4.14. For the smaller tuning range compared to VCOs, FFOs need to be designed with less flexibility to parasitic variations. A negative-resistance oscillator using SiGe HBT is optimized and implemented in IBM 0.18 μm SiGe-BiCMOS process. A CMOS cross-coupled oscillator is designed optimizing the interconnect parasitics using 130 nm NMOS devices, and two versions of this oscillator are fabricated.

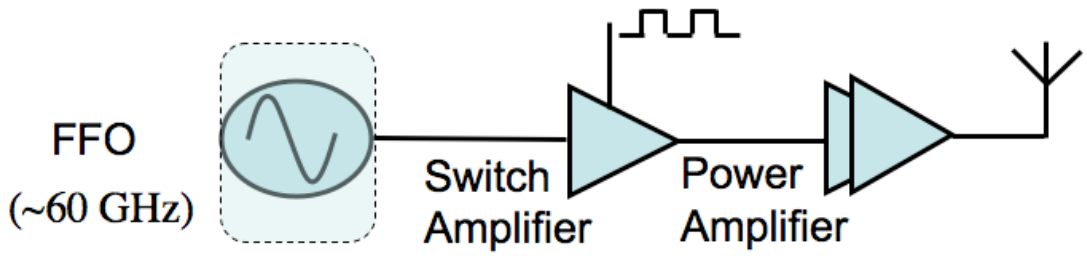
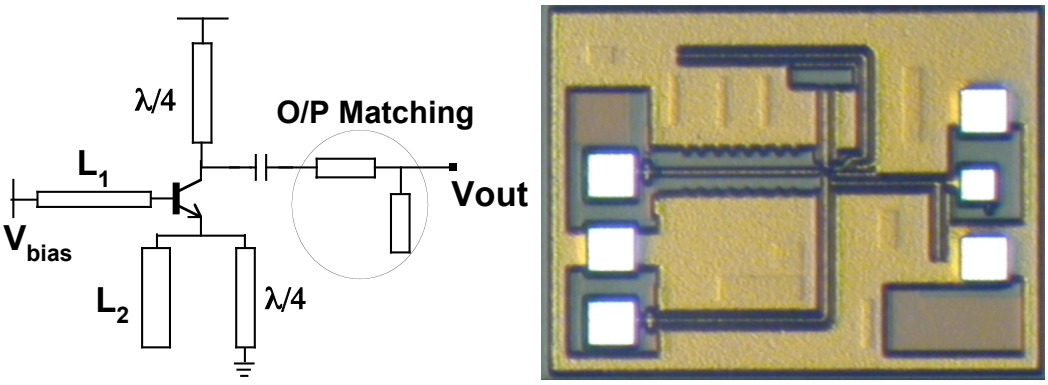


Figure 4.14. The block diagram of the ASK transmitter.

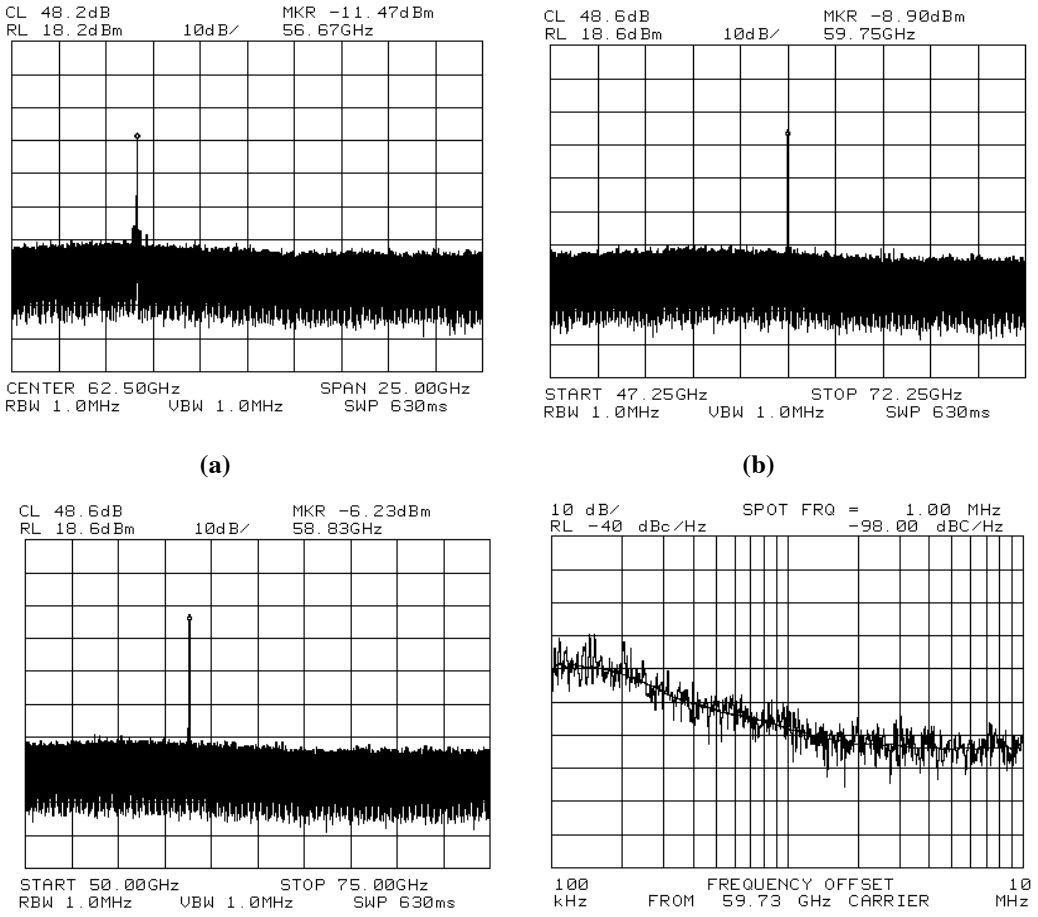
4.4.1.1 SiGe 60 GHz negative-R oscillator

The oscillations at 60 GHz are realized using negative-resistance topology in common-emitter (CE) configuration. Micro-strip line inductance at base and open stub capacitances at the emitter are used to provide negative resistance in CE configuration. Both these components provide the instability required to start the oscillations. The schematic is shown in Figure 4.15a, and the die photograph is shown in Figure 4.15b. Three different versions of the same topology with different lengths of micro-strip line lengths are fabricated, and their center frequencies are measured to be 56.7 GHz, 58.7 GHz, and 59.7 GHz respectively. The measurement results of the oscillators are summarized in Table 4.1. The layout is mostly transmission-line-based (type 2, as shown in Figure 4.4), and hence, the effects of parasitics for a compact layout is found to be <10% i.e. less than 6 GHz. The oscillation frequency is more dependent on the active device large-signal characterization and transmission-line models. Also, the interconnect effects are reduced for using a HBT device length of only 6 μm as the oscillation device. The measured output spectrums for the oscillators are shown in Figure 4.16a and Figure 4.16b respectively. The best-achieved phase noise performance is around -98 dBc/Hz at 1 MHz offset as shown in Figure 4.16c.



(a) (b)

Figure 4.15. (a) The schematic and (b) the die photograph of the 60 GHz oscillator.



(a) (b)

(c) (d)

Figure 4.16. (a), (b) &(c) The measured spectrum of the oscillators (total loss = 4dB). (d) The phase-noise performance at 59.73 GHz oscillation-frequency.

Table 4.1. Measured performance of the oscillators

Center frequency	56.8, 58.8 and 59.8 GHz
DC power consumption	6-10 mW
Power supply	1.2-1.6V
Output power	-7 to –3.5 dBm
Frequency range	1-1.2 GHz
Phase noise	-98 dBc/Hz @1MHz offset

4.4.1.2 CMOS oscillators at 60 GHz

Cross-coupled oscillators are designed using 130 nm NMOS devices available in 0.13 μm SiGe-BiCMOS process from IBM Corporation. Oscillation frequencies very close to the f_T (around 90-100 GHz) of these devices are targeted to understand the effects of parasitics close to the technology limits. Two versions of oscillators are designed around 65 GHz with different lengths of the tuning micro-strip (MS) line. The schematic with parasitic components is shown in Figure 4.17. The output power at these frequencies is maximized with accurate optimization of parasitics. The die photograph for one of the oscillator test structures is shown in Figure 4.18. The measured results for different versions are presented in Figure 4.18. The spectrum and phase noise performance for the 63-GHz oscillator (version 1) are shown in Figure 4.19. The measured performances for the 66-GHz oscillator (version 2) are shown in Figure 4.20. The measured frequency is within 3% of the estimated oscillation frequency including layout parasitics.

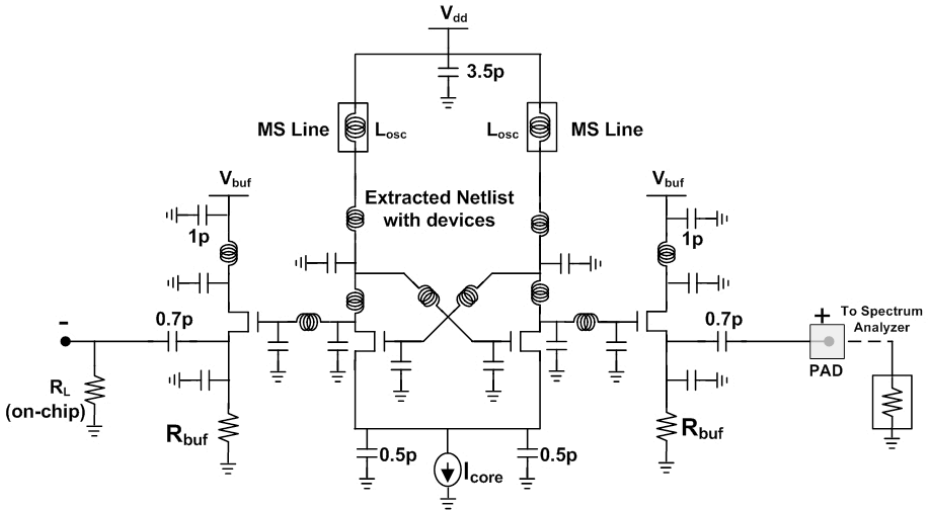
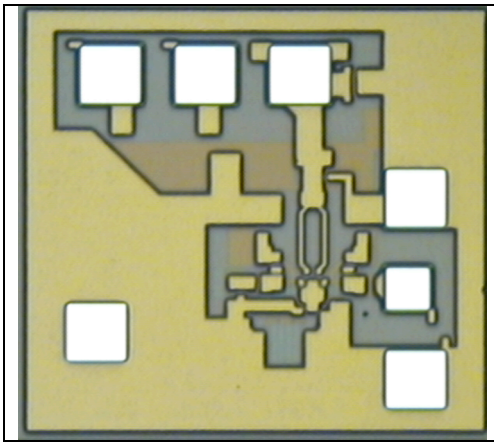


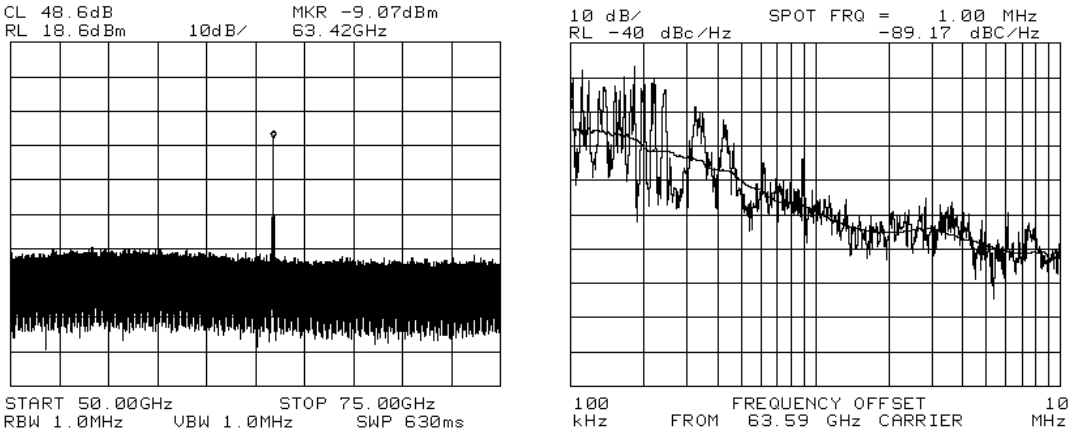
Figure 4.17. The schematic of the CMOS fixed-frequency oscillators.



Measured results (Version 1/Version 2):

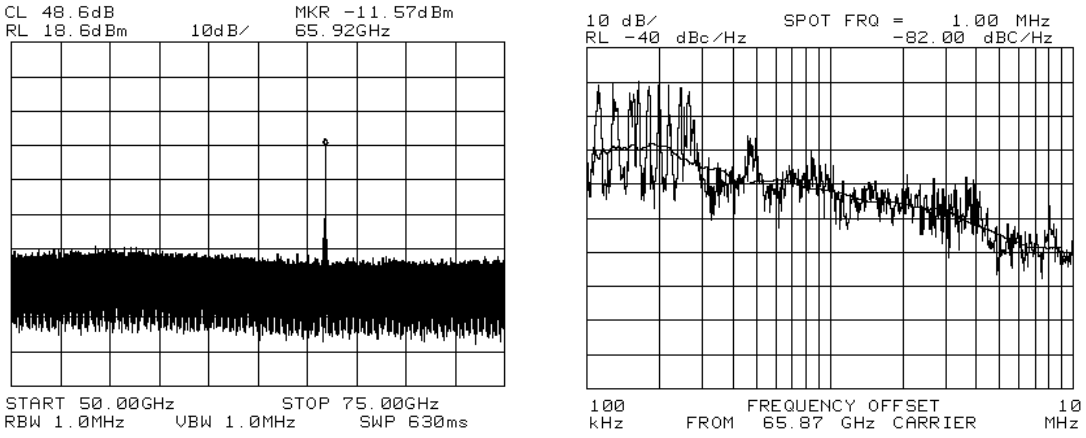
Center frequency= 63.4 GHz/ 66 GHz
Tuning range= 1-1.5 GHz (varying DC conditions)
Power supply =1.5 Volt.
Power consumption=25 mw (core + buffer)
Output power = - 5 to -8 dBm
Best phase noise >-90dBc/Hz @1MHz offset

Figure 4.18. Die photograph and performance table for the CMOS oscillators.



(a) **(b)**

Figure 4.19. (a) The measured spectrum of the oscillators (total loss = 4 dB) and (b) The phase-noise performance at 63.6 GHz oscillation-frequency.



(a) **(b)**

Figure 4.20. (a) The measured spectrum of the oscillators (total loss = 4 dB) and (b) The phase-noise performance at 65.9 GHz oscillation-frequency.

4.4.2 VCO examples

In this subsection, different VCO examples are presented with oscillation frequencies varying from 10 GHz to 55 GHz in silicon-based processes. Cross-coupled, push-push and quadrature-generation topologies are investigated, and the effects of parasitics are demonstrated. A SiGe cross-coupled oscillator is designed, and the layout complexities are compared to a CMOS cross-coupled oscillator. A CMOS push-push VCO at 50 GHz and a cross-coupled VCO at 45 GHz are designed using the parasitic benchmarking procedure that is developed in section 3.4 in the third chapter. The difference between parasitic sensitivities for using different topologies to generate frequencies in the same range is described. Later, a quadrature VCO at 8-10 GHz is designed as the VCO#2 considering the super-heterodyne architecture as shown in Figure 4.1 and 4.2.

4.4.2.1 SiGe cross coupled VCO

A cross-coupled VCO is designed targeting 30 GHz center frequencies. Figure 4.21 shows the schematic of the cross-coupled core. A DC blocking capacitor is used to complete the cross-coupled loop. Most of the added parasitics come from the requirement

of this capacitor in contrary to a CMOS cross-coupled core where the drain voltages can be directly fed to the gates. There are additional parasitic components due to connections between metal layers used in the active device and the top metal layers used in capacitors and micro-strip lines. The values of DC blocking capacitor (C_{dc}) and the varactor dimensions are important to optimize the parasitics as well as to meet the bandwidth requirements.

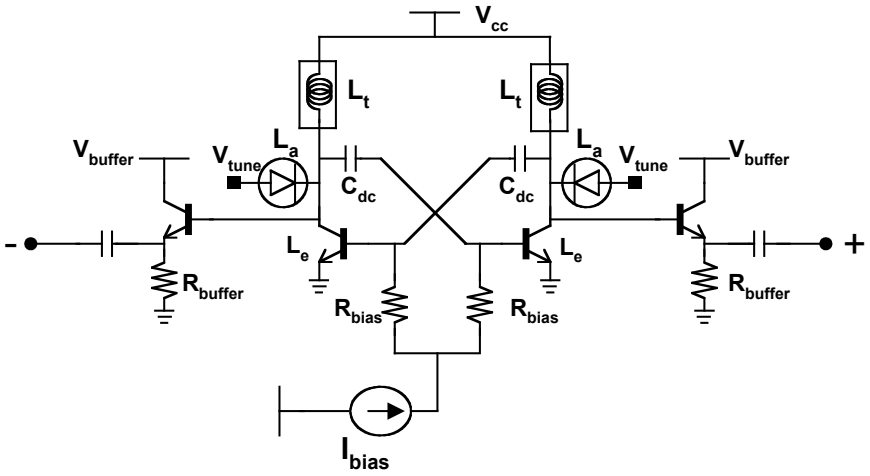


Figure 4.21. The schematic of the 30 GHz VCO.

Emitter-follower buffers are used to deliver the output power to a 50-ohm load and to provide isolation from the load. One of the differential outputs is terminated using a 50-ohm on-chip resister. The power consumption of the cross-coupled core is 10 mW and that of buffer is 5-10 mW. Three different versions, varying length L_t of the tuning micro-strip line, are implemented to have center frequencies 29,31 and 33 GHz with estimated parasitic matrix. The simulated tuning range is around 2.5 GHz. The power supply used for cross-coupled core is 1.4V and that for buffer is 1.8V. The $2^{nd}/3^{rd}$ harmonic distortion is less than -30 dBc. The layout is shown in Figure 4.3 as an example of pad-dominated layout (type 1). The detailed layout optimization and parasitic sensitivity analysis of cross-coupled SiGe- HBT VCOs will be presented in the next chapter (section 5.1).

The die photograph of one of the VCOs is shown in Figure 4.22a. The tuning characteristics are shown for three different tuning inductance lengths (L_t =160, 175 and 190 μm) in Figure 4.22b. The center frequencies are within 500 MHz compared to the predicted oscillation frequencies. The VCO test structures show maximum power output of -3 dBm (shown in Figure 4.22c) with 15-20 mW DC power consumption, linear tuning range of 2.3-2.7 GHz, and best phase noise performance as -98 dBc/Hz @1MHz offset shown in Figure 4.22d. The cross-coupled core with buffer takes a die-space of only 300 x 300 μm^2.

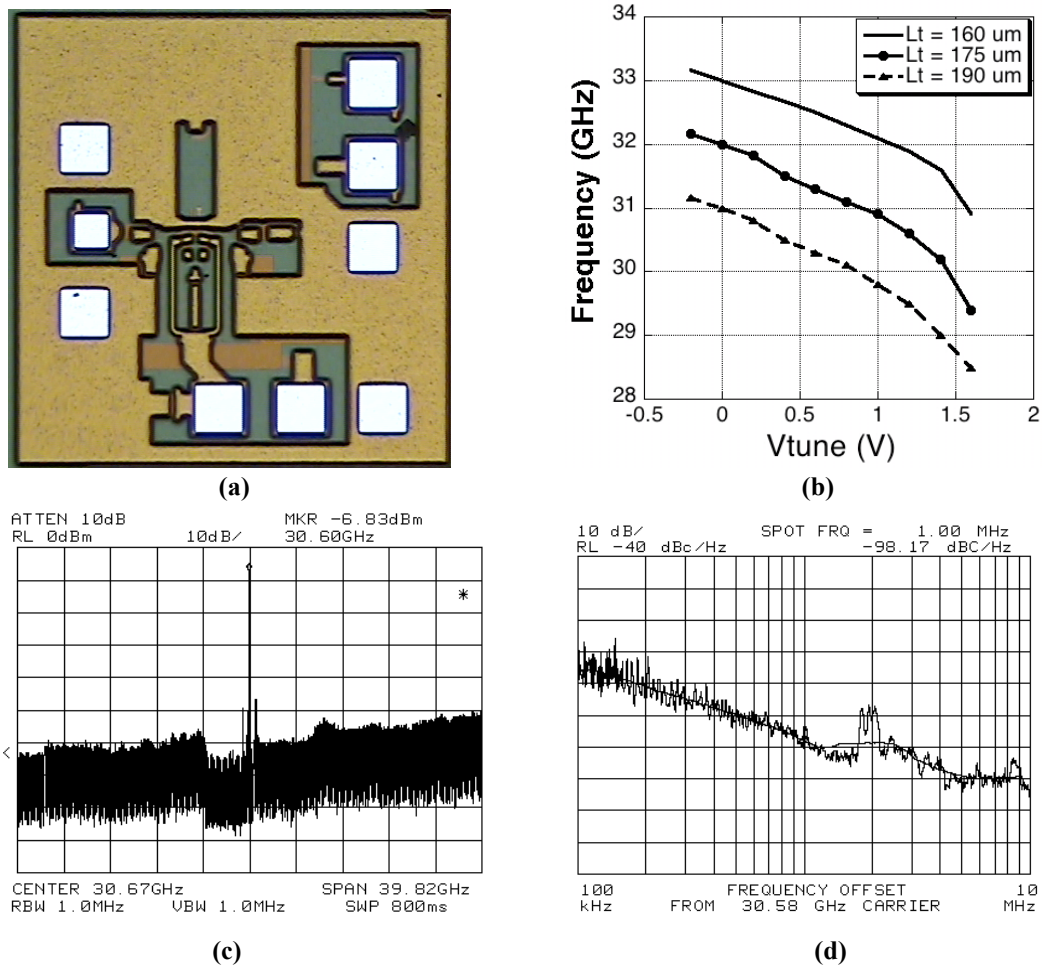


Figure 4.22. (a) The die photo, (b) the tuning characteristics, (c) the output spectrum, and (d) the phase noise performance of the VCO.

4.4.2.2 CMOS push-push VCO

Push-push oscillation topology is realized by a cross-coupled pair with the common node at the tuning inductance sides being connected to a quarter-wavelength stub at the desired frequency given the cross-coupled core oscillates at half the required frequency. The schematic is shown in Figure 4.23. In this work, a push-push VCO (with varactor) is designed around 50 GHz to be used in a super-heterodyne architecture for 60 GHz applications. The oscillation devices used are 20μm width devices with 20 fingers in a 90 nm CMOS technology. The varactor used has a varying capacitance of 50-100 fF for higher frequency tuning range. Using parasitic benchmarking procedure developed from oscillator (without varactor) measurements in section 3.4, the VCO center frequency is predicted to be around 52 GHz with ~5 GHz/V tuning gain. The measured oscillation frequency is within 1% of that predicted by the analysis. The measured results for four different chips are shown in Figure 4.24. The results are taken for different chips under same DC conditions. The current consumption of the core is 15-20 mW, and that for buffers is 6-12 mW. The maximum output power obtained at 25-GHz- and 50-GHz-ports are -5.5 dBm and -8.8 dBm respectively for 50-ohm terminations. The die photo is shown in Figure 4.25. The measured results are presented in Table 4.2.

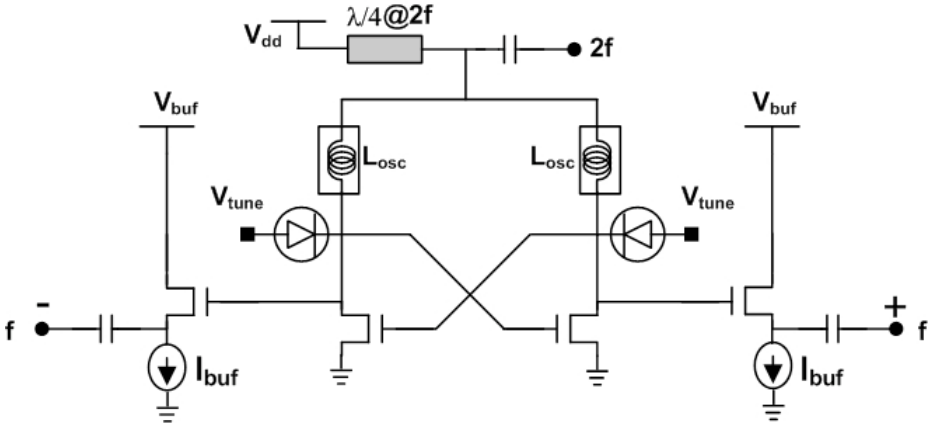
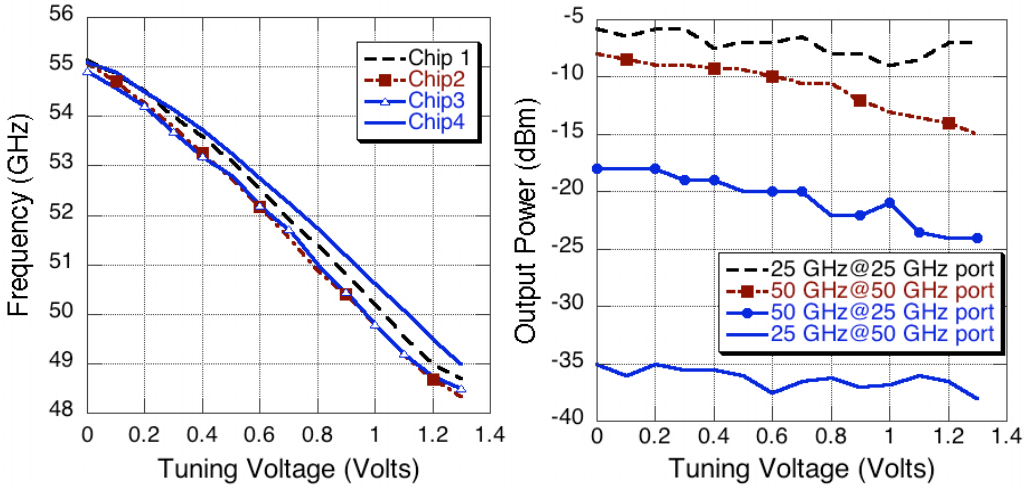


Figure 4.23. The schematic of the push-push VCO.



(a) **(b)**

Figure 4.24. The measured performances of the push-push VCO.

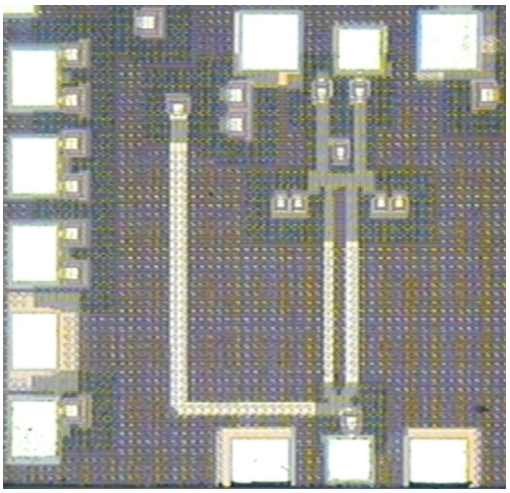


Figure 4.25. The die photo of the push-push VCO. ***[Simulated phase noise!]***

Table 4.2. The simulation to measurement comparison

Simulated results:	**Measured results:**
Frequency: 49-54.6 GHz, Tuning Gain (K_{VCO}) = 4.4 GHz/V Output power @ cross-coupled output i.e. 25-GHz port = - 6 dBm Output power @ push-push output i.e. 50-GHz port for 50-ohm terminations = - 12 dBm	Frequency: 49-55 GHz, Tuning Gain (K_{VCO}) = 4.7 GHz/V Power consumption=25-30 mW(core + buffer) Output power @ cross-coupled output i.e. 25-GHz port = - 5.5 to -8 dBm Output power @ push-push output i.e. 50-GHz port = - 8.8 to -13 dBm Phase noise > -90 dBc/Hz @1 MHz offset

4.4.2.3 CMOS cross-coupled VCO

A cross-coupled oscillator is designed to generate ~45GHz signal for verifying the parasitic benchmarking procedure developed in section 3.4 using 90 nm CMOS process. The oscillation devices used are 20µm width devices with 20 fingers. The oscillation frequency is within 2% of that predicted by the analysis. The varactor used is small (varying capacitance 35-65fF) for reliable oscillations. The schematic and control characteristics are shown in Figure 4.26 and 4.27 respectively. The die photo and measured results are presented in Figure 4.28.

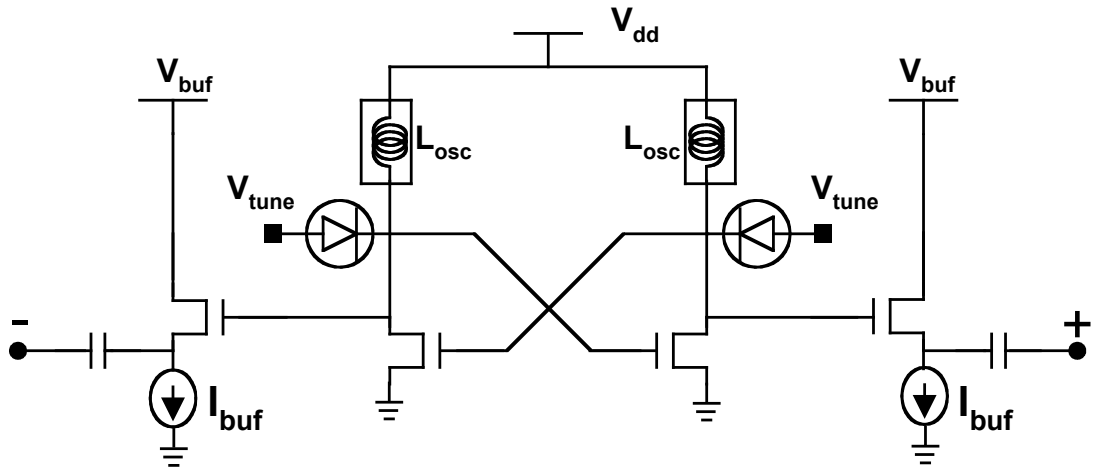


Figure 4.26. The schematic of the cross-coupled VCO.

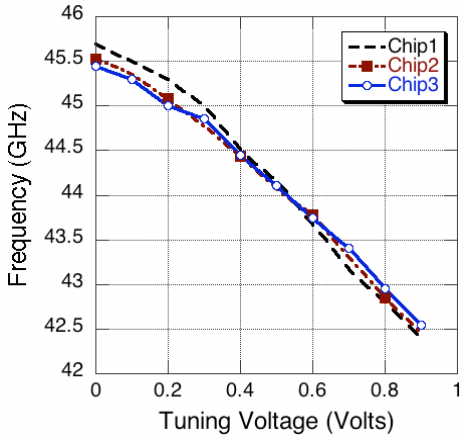
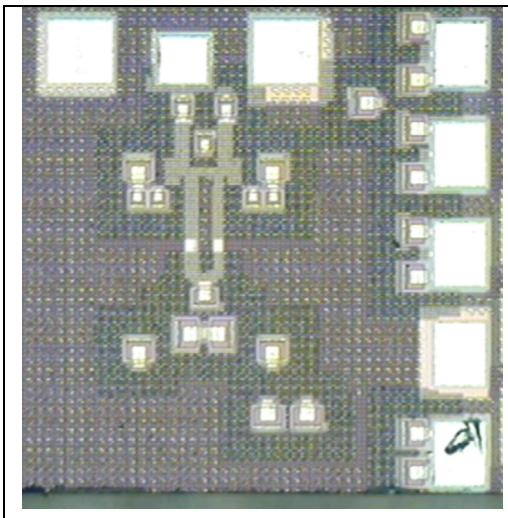


Figure 4.27. The control characteristics of the cross-coupled VCO.



Simulated results:

Frequency: 43.2-46 GHz,
Tuning Gain (K_{VCO}) = 3.1 GHz/V
Output power at 50-ohm termination = - 7 dBm

Measured results :

Frequency: 42.5-45.5 GHz,
Tuning Gain (K_{VCO}) = 3.3 GHz/V
Power consumption=15-20 mW(core + buffer)
Output power = - 5 to -9 dBm

Phase noise > - 90 dBc/Hz @1 MHz offset

Figure 4.28. Die photograph and performance table for the cross-coupled VCO.

The push-push topology has its advantages over cross-coupled pair for its lower frequency of oscillation at the cross-coupled pair. Also, the use of frequency dividers at 50 GHz input frequency can be avoided while realizing an integrated VCO-PLL. The parasitic shifts in frequency are 10-15% compared to 20-30 % shifts in a direct cross-coupled realization of 50 GHz oscillations in a 90 nm CMOS process. But the 3-6 dB lower power-outputs in push-push oscillators make it difficult to integrate them with mixers that demand higher LO power. Also the layout is more compact in cross-coupled topology that can be realized without the quarter-wavelength stub and shorter tuning lines.

4.4.2.4 CMOS QVCO

Quadrature signal generations are necessary in base band to modulate/demodulate signals in QPSK/QAM schemes. Considering a super-heterodyne architecture, a quadrature VCO (QVCO) has been implemented to understand the parasitic effects at these frequency ranges. The schematic of the QVCO is shown in Figure 4.29. The major

parasitics are included in the design, and the percentage shift is confirmed from measurement results. The feedback lines between the cross-coupled cores contribute most in the shift in frequency. Other dominant parasitic components are the connections between active devices and the large inductors/varactors. But the percentage shift due to parasitics is less than 10% compared to the shift of up to 30% for oscillators with oscillation frequencies above 30 GHz. The measured tuning characteristics are shown in Figure 4.30. The die photograph and measured results are summarized in Figure 4.31.

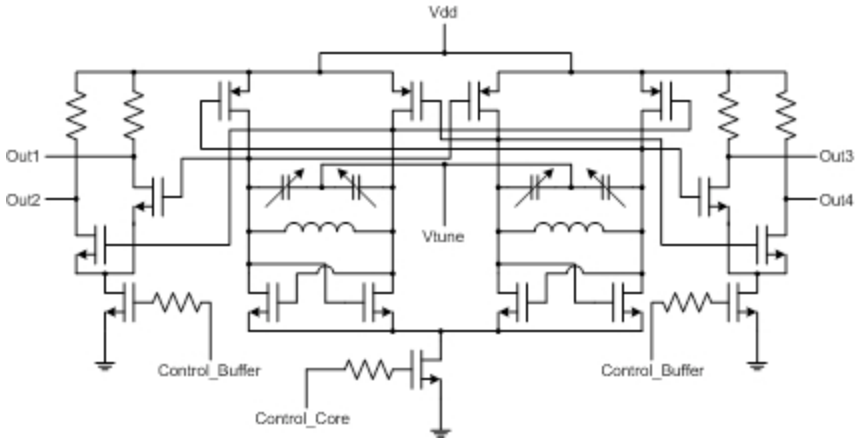


Figure 4.29. Schematic of the preliminary QVCO.

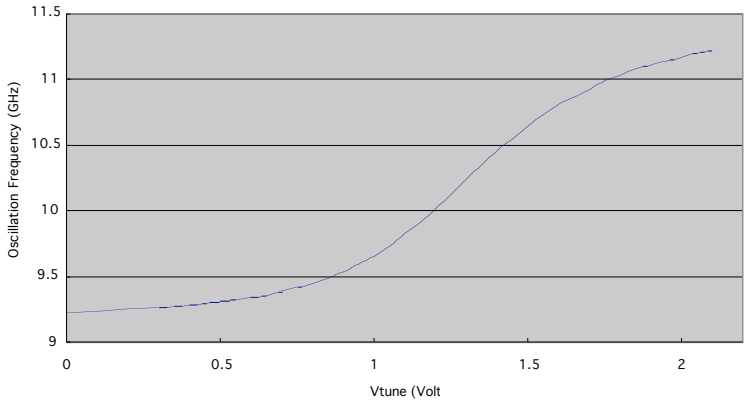
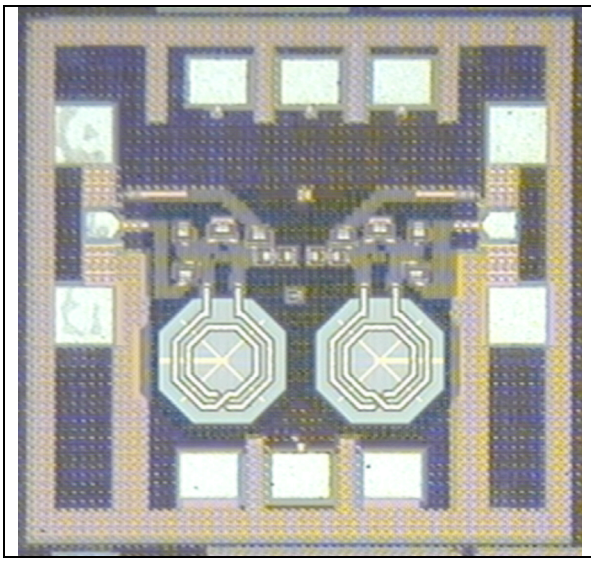


Figure 4.30. Measured Tuning Curve of the preliminary QVCO.



Measured results :

Frequency: 9.9 GHz
Linear tuning range: ~ 1 GHz
Power consumption: 19.6 mW,
Phase Noise: better than -90 dBc @1 MHz offset
Output power: -16 dBm using 50 Ohms load; equivalent to 780mV peak-to-peak on Mixer capacitive load.

Figure. 4.31. Die photograph and measured performances of the preliminary QVCO.

4.4.3 Frequency dividers

Frequency dividers are critical blocks for a VCO with integrated PLL. For an integrated transceiver, PLLs need to be used to reduce the phase noise as well as to generate a very accurate frequency. There are mainly two types of dividers for frequencies higher than 10 GHz. They are injection-locked dividers and master-slave flip-flop-based dividers. In this subsection, the second type is studied to demonstrate the parasitic effects.

Four different test structures are measured to determine divider operating ranges. Three of them are designed to operate around 25 GHz as divide-by-512 block with different device widths. These divider chains include three master-slave flip-flop (FF) based dividers, and rest six stages are Dflipflop (DFF)-based dividers. One more divider chain is designed to operate as divide-by-256 block around 10 GHz. This divider has two master-slave-FF-based and six DFF-based stages. The block diagram representation of the divider chains is shown in Figure 4.32. The device widths for cross-coupled pairs in

the 1st stages of the 25-GHz divider blocks vary between 2 to 2.4μm with two fingers. The device widths for cross-coupled pairs in the 1st stage of 10-GHz divider and the 2nd stages of 25-GHz divider blocks vary between 5 to 6.5μm with multiple fingers.

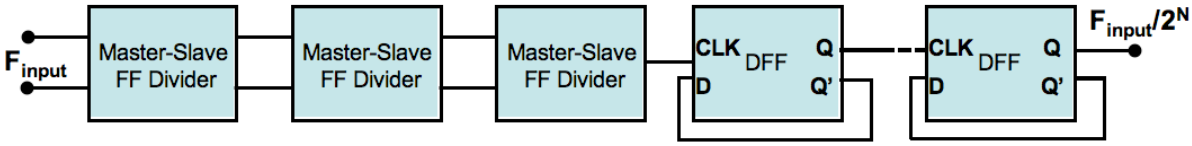


Figure 4.32. The block diagram of the divider chain.

The schematic for the Dflipflop-based divider is shown in Figure 4.34. The DFF-based dividers work for digital signals, and hence they work till a certain frequency for a fixed input swing. The figure of merit is defined as the product of functionality factor (1 if dividing, 0 otherwise) and the output voltage swing. The figure of merit is plotted with and without parasitics for input frequency variations in Figure 4.34. The maximum operating frequency for 0.8 Volt swing is reduced to 3.6 GHz from 6 GHz due to parasitics. The layouts of these two dividers are shown in Figure 4.35a and Figure 4.35b respectively.

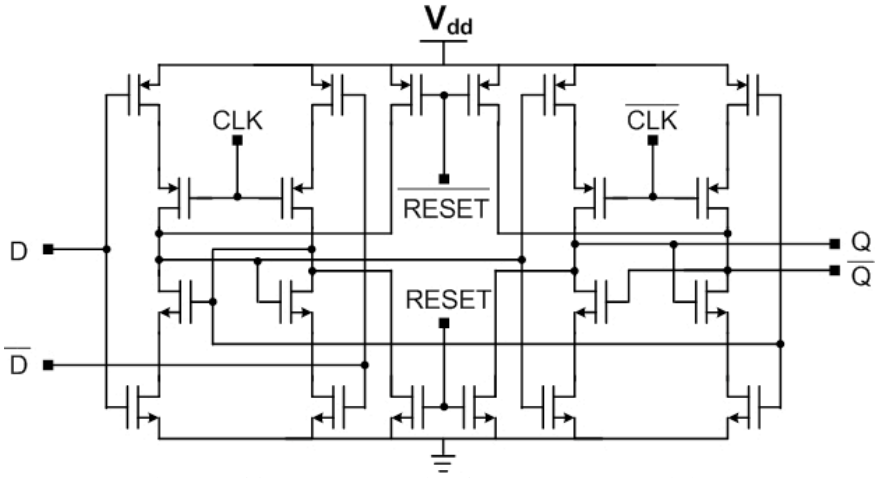


Figure 4.33. The schematic of the DFF-based divider.

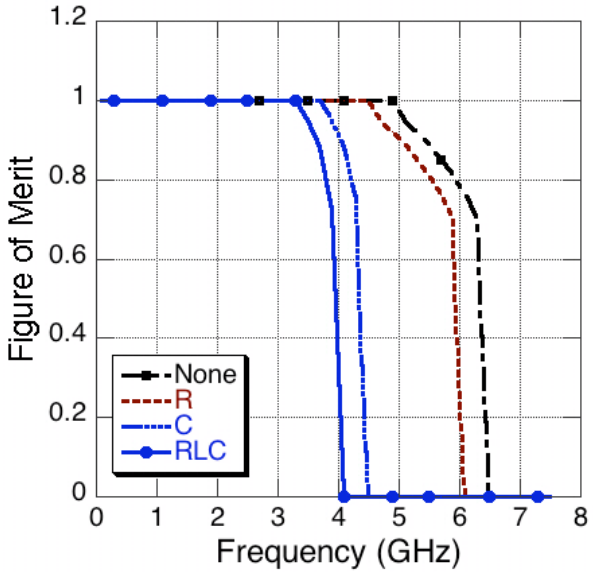
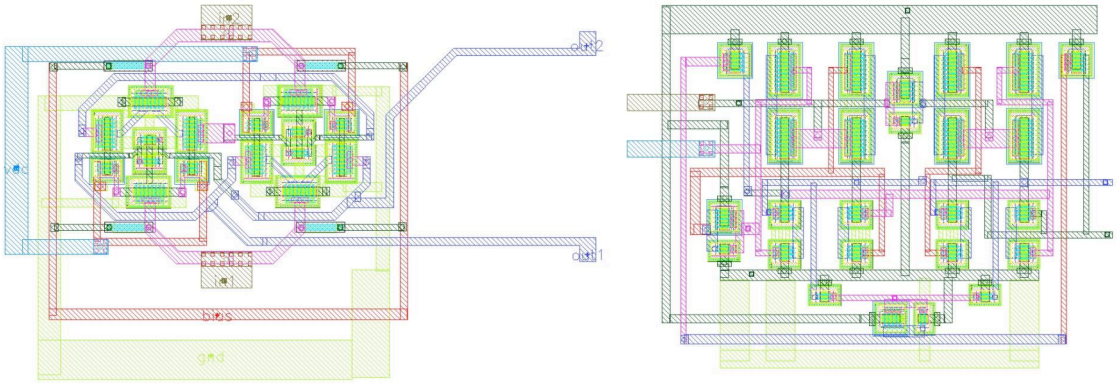


Figure 4.34. The simulated performances of DFF-based dividers with and without parasitics.



(a) **(b)**

Figure 4.35. The layout of master slave FF-based and DFF-based dividers.

The schematic for the master-slave FF divider with the parasitic components is shown in Figure 4.36. The cross-coupled pairs decide the self-resonating frequency and hence, the deep of the frequency sensitivity range. A PMOS load [4.10] is used to provide the gain for differential amplifier stages. It is clear that the first two stages decide the division range for the whole divider chain.

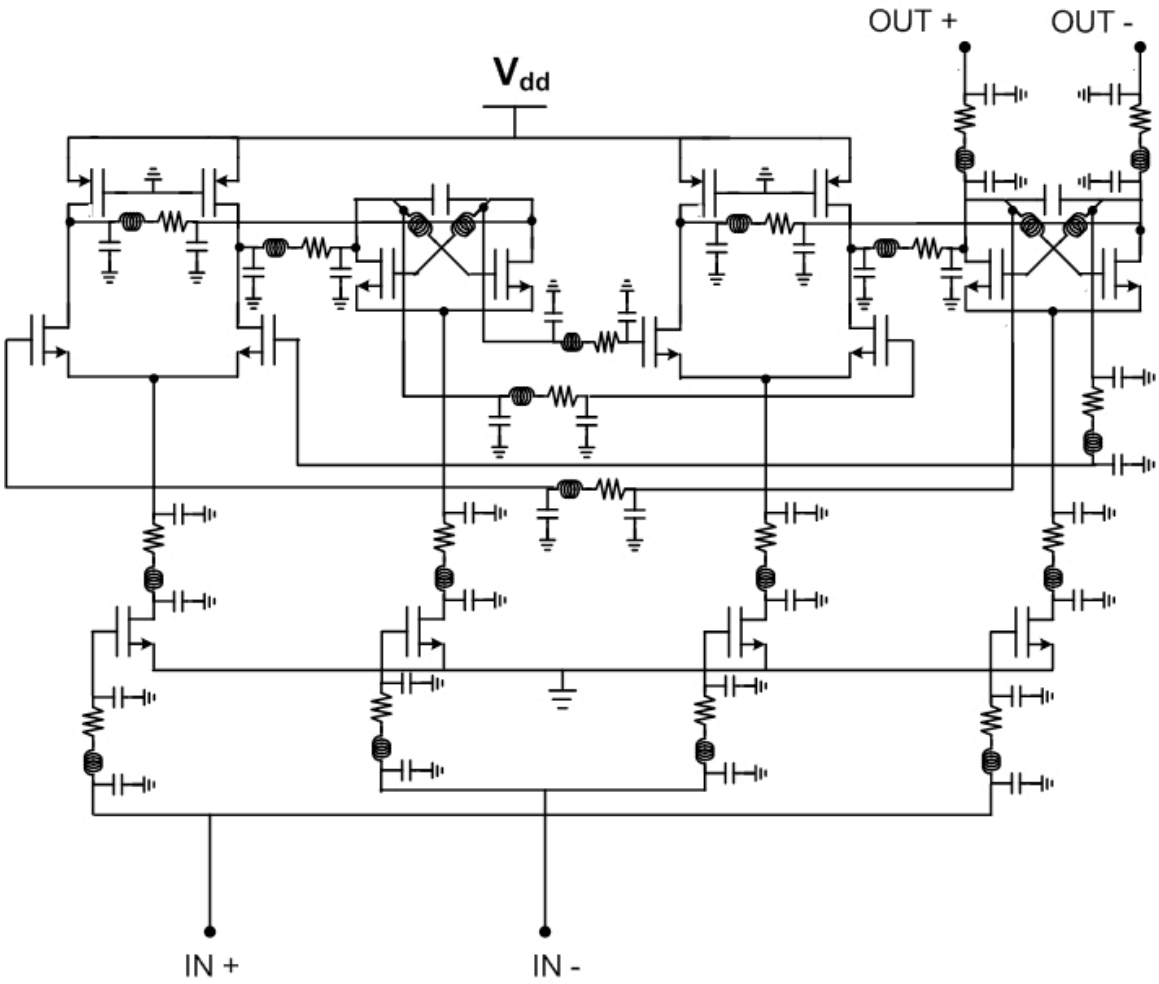


Figure 4.36. The schematic of the master-slave FF-based divider with parasitics.

The variations of frequency sensitivity curves with parasitics are shown in Figure 4.37. The parasitic effects on individual divider stages are summarized for different dividers in Table 4.3. While evaluating the frequency range of division, the load of the next stage is included in the simulation. From the frequency ranges, it is clear that the lower cut off is downshifted much lesser than the upper cutoff frequencies for more pronounced parasitic effects at higher frequencies. Also, the shifts in operating frequency ranges are sometimes more significant in 2^{nd} stages of the dividers chains because bigger devices are used to achieve lower resonant frequencies.

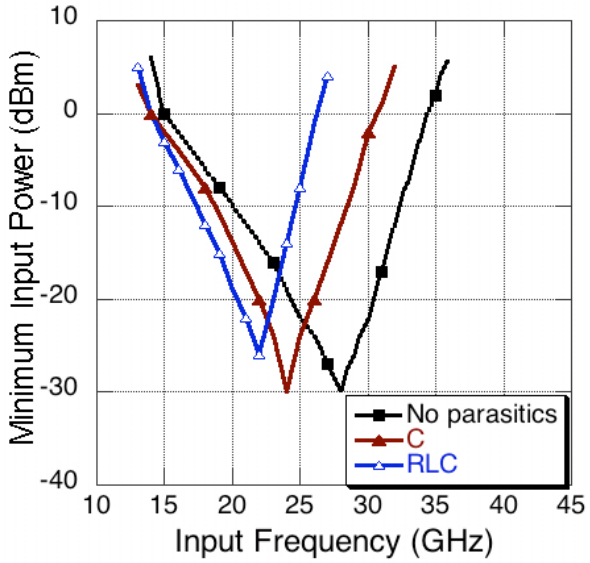


Figure 4.37. The simulated frequency sensitivity curves with and without parasitic effects for one of the divider-chains (divide by 512).

Table 4.3. The parasitic effects on divider stages

Frequency range of division	Without parasitics	Including RLC networks
1st Stage for divide-by-512 (version 1)	14-36 GHz	13-27 GHz
1st Stage for divide-by-512 (version 2)	16-39 GHz	13-29 GHz
2nd Stage for divide-by-512 (version 1)	6-19 GHz	5-14 GHz
1st Stage for divide-by-256	5-15 GHz	4-11 GHz
DFF-based divider	0.1-6 GHz	0.1-4.5 GHz

The die photo of the divider chains is shown in Figure 4.38. The measured divider sensitivity curves for different dividers are shown in Figure 4.39 for two different dies. The power supply is fixed to 1.4V. The self-oscillating frequency increases with increasing power supply. The measurement results are summarized in Table 4.4. As shown in Figure 4.39b, the different percentage shifts in first two stages may significantly reduce the operating range of the divider chain. The shifts in the operating frequencies

from the simulation including parasitics are due to modeling shifts for PMOS loads, and it can be removed using resistive or NMOS loads instead of PMOS loads.

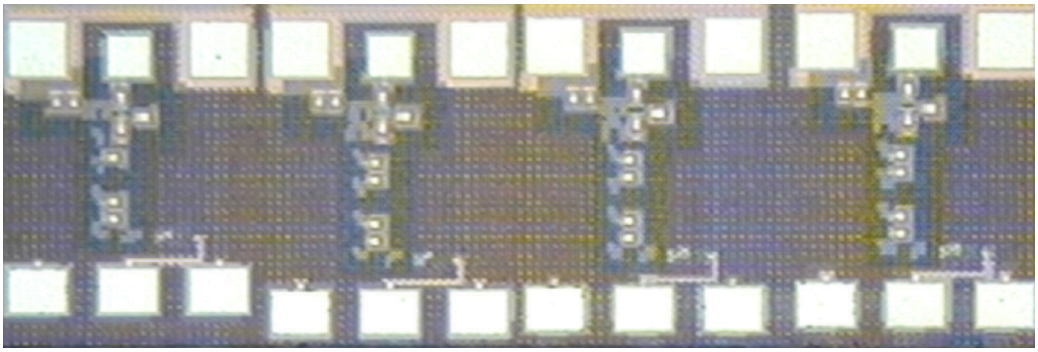


Figure 4.38. The die photo of the divider test structures.

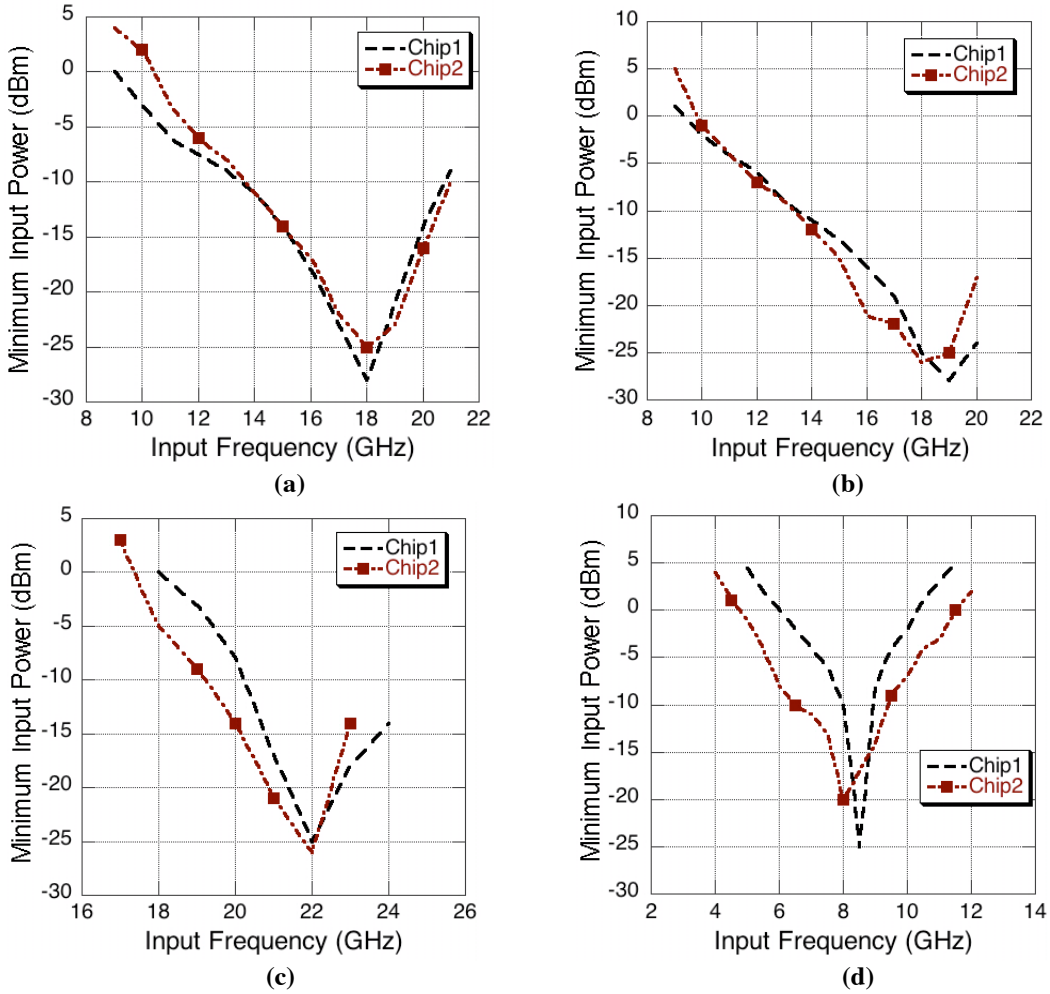


Figure 4.39. The measurement results of the dividers.

Table 4.4. The measured performance of the divider chains

Performance Parameter	25GHz Divider, version 1	25GHz Divider, version 2	25GHz Divider, version 3	10GHz Divider
Frequency Range@0 dBm	10-21 GHz	10-20 GHz	17.5-23.5 GHz	4.5-11.5 GHz
Self-resonating Frequency (1st Stage)	18.6 GHz	19.6 GHz	22.1 GHz	8.4 GHz
DC Power Consumption	18 mW	18 mW	15 mW	13 mW

4.4.4 Amplifiers

As explained earlier, amplifiers at millimeter-wave frequencies are mostly designed using measurement results from transistors and transmission lines. Thus, the requirement of a detailed parasitic analysis is less, and the results are more dependent on the device models developed. The intrinsic/extrinsic parasitics for the transistors should be accounted in the measurement-based models. However, the interconnect- and off-chip-parasitics at certain nodes may be critical for amplifiers. Two such cases are demonstrated using low-noise-amplifier (LNA) and power-amplifier (PA) examples.

4.4.4.1 Low noise amplifier

A cascode amplifier using 180 nm SiGe-HBT devices is studied as a low noise amplifier. The schematic of the low noise amplifier is shown in Figure 4.40a. The inductive parasitic component is considered for the cascode core as shown in Figure 4.40b. The inductance (L) is capable of boosting the gain [4.11] of the amplifier as shown in the maximum available gain (MAG) plots in Figure 4.40c.

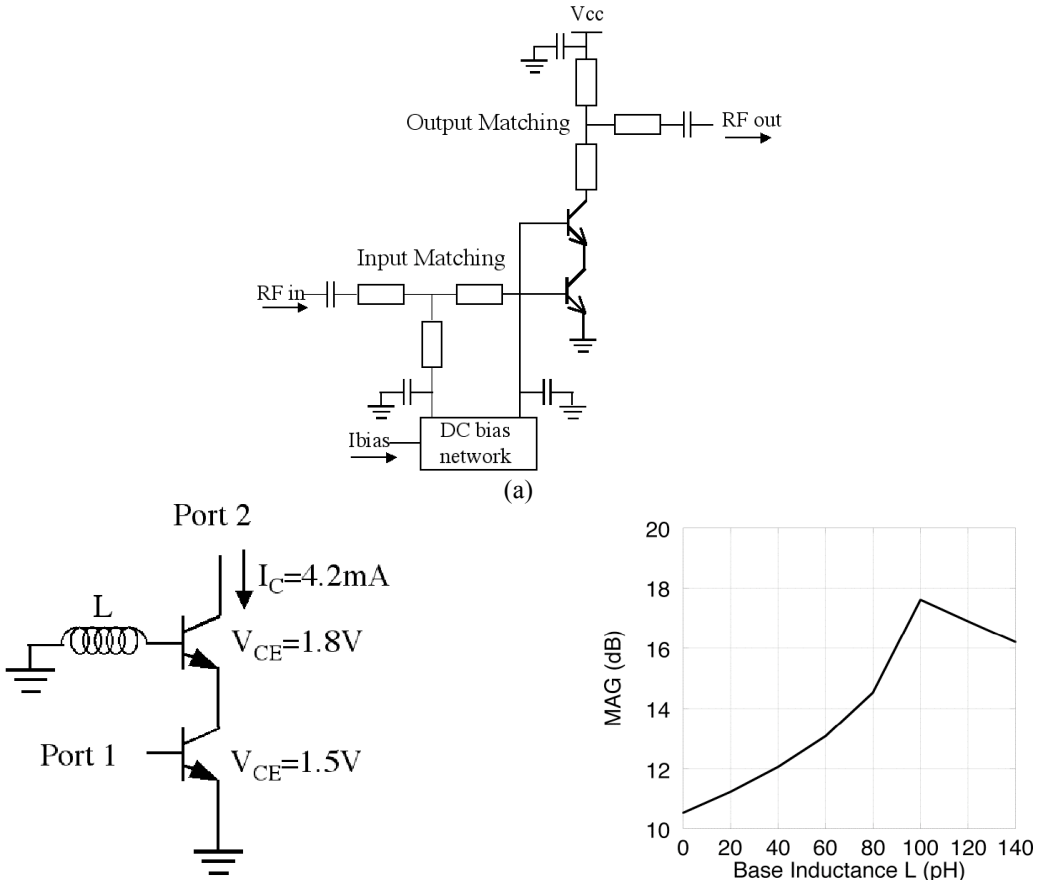
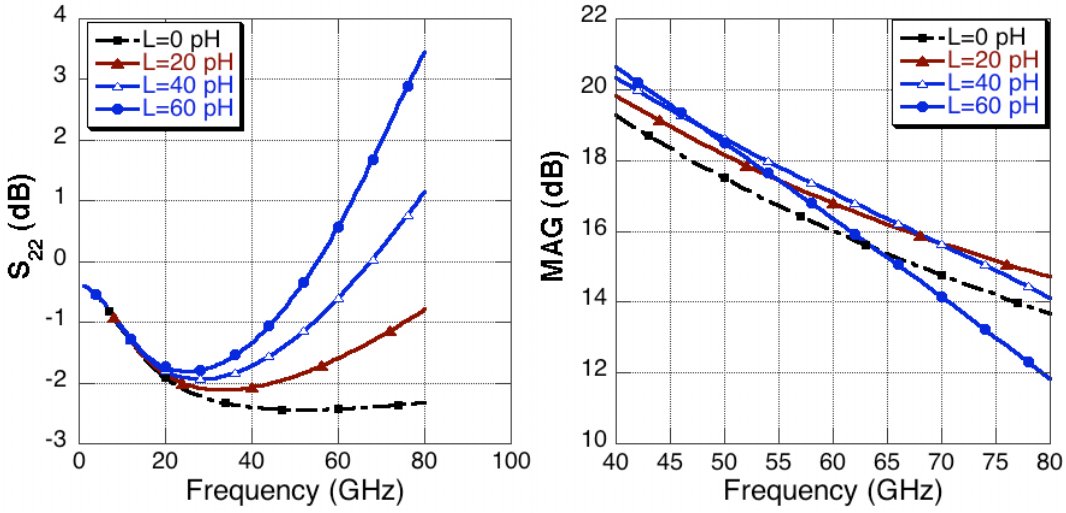


Figure 4.40. (a) Schematic of the cascode core; (b) MAG of casocode core with base inductance (*L*).

The inductance (L) decreases the real part of the looking impedance of the CB stage thus decreasing the stability of the circuit. Hence, with higher inductive components at that node, the amplifier will go unstable. The effects in CMOS amplifiers are more pronounced. In Figure 4.41, the effects of the gate inductance on output matching (i.e. S_{22}) and the maximum available gain (MAG) are shown for a 90 nm cascode LNA. The greater than 0 dB values of S_{22} at higher frequencies signify instability.



(a) (b)

Figure 4.41. The effect of gate inductance on (a) output matching (S_{22}) and (b) maximum available gain for the cascode LNA.

4.4.4.2 Power amplifier

For power amplifiers, the stability of the amplifier is a critical issue since devices with larger widths are used, and two or more stages are cascaded to meet the gain requirements. The effects of on-chip parasitics in the layouts of power cells are already described in section 2.3. In Figure 4.42, the measurement set up for a power amplifier is shown. The DC probe inductance will be replaced by wire-bonding inductance or package parasitics in a package/module implementation.

To show the effects of this inductance, a SiGe HBT amplifier is studied as shown in Figure 4.42. The variations of S_{22} (output matching) with different values of probe inductance are shown in Figure 4.43a. For a fixed inductance of 500-pH value, the effects for different values of de-coupling capacitors are shown in Figure 4.43b. The effects are usually more pronounced for active devices with higher gain. The amplifiers can be stabilized by reducing the current consumption and hence, decreasing the transducer gain in high-gain stages.

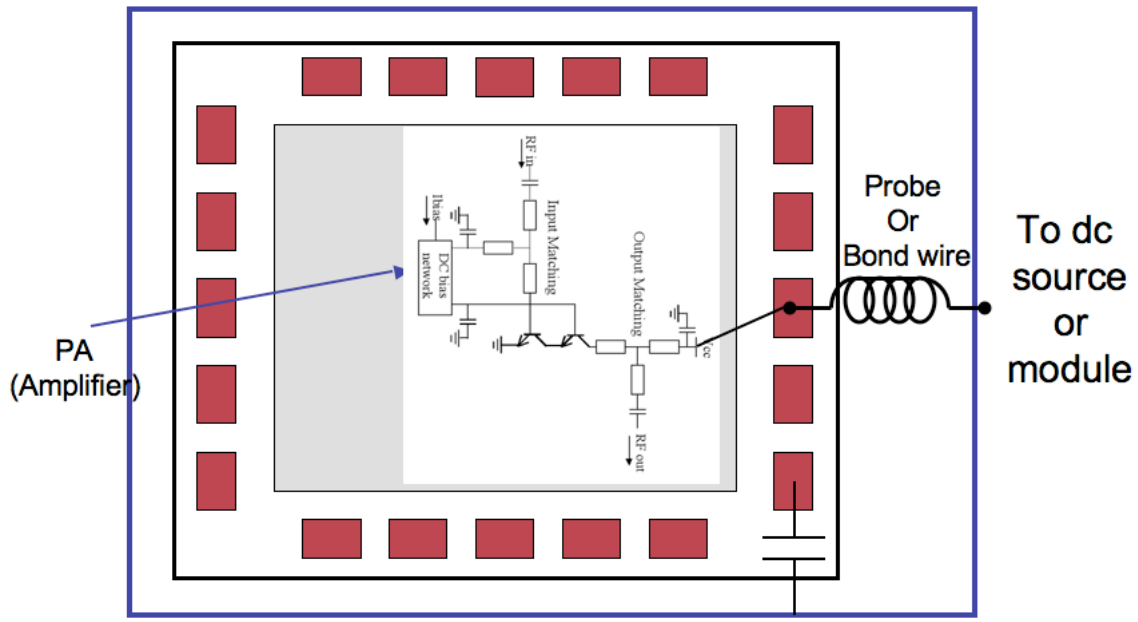
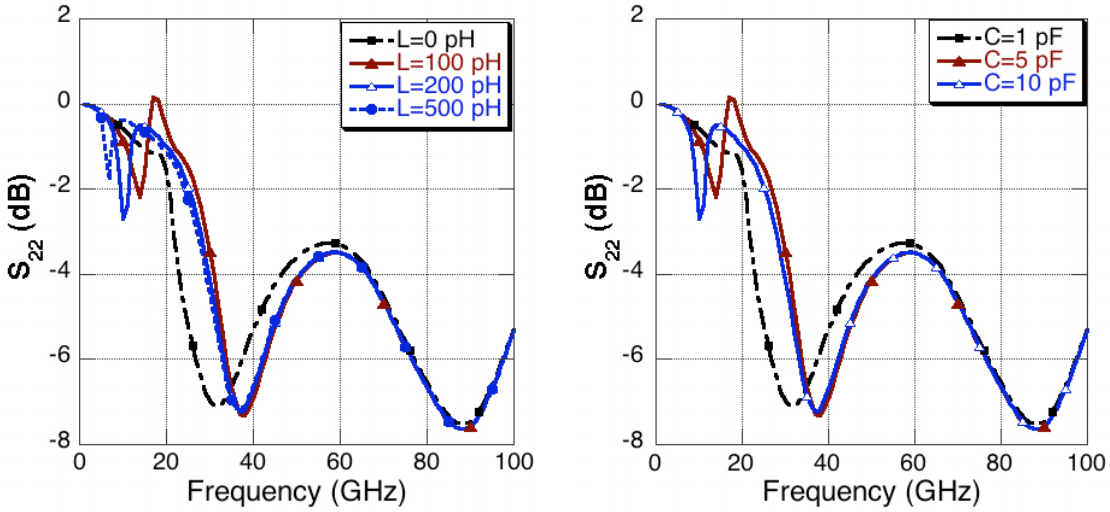


Figure 4.42. The presence of probe or bond-wire inductance in the measurement/ implementation setup for amplifiers.



(a) **(b)**

Figure 4.43. The effects of (a) probe/bond-wire inductances and (b) de-coupling capacitors on the output matching (S_{22}) for the SiGe one stage PA.

4.5 Important issues related to parasitics at MMW frequencies

There are some common issues related to parsitics that can be applied to all MMW circuits. In this sub section, two of them i.e. effects of substrate and process variations are described.

4.5.1 Substrate effects

Substrate parasitics can no longer be neglected for giga-hertz operations. The extraction of substrate resistance is very important for mainly two reasons. Firstly, around the active devices, the substrate resistance changes the device performances at high frequencies. Secondly, in the layout, the effects of interconnect capacitances to substrate depend on how substrate is connected to global ground. For a metal signal line without any defined ground, the capacitance is between signal and substrate. If substrate is kept open, the substrate capacitance effects will be minimal. On the other hand, if substrate is connected to ground using a large number of contacts or via holes, the effects of parasitic capacitances will be significant.

Since, the substrate resistance is a distributed resistance that depends on substrate doping, number of tap connections as well as distance from global grounds, it is difficult to estimate them [4.12, 4.13]. An intuitive way to solve the problem is to determine the substrate potentials, dividing chip area into small rectangles, depending on substrate contacts, guard rings around devices as well as the final system-ground definition. Accordingly, a substrate network will model every region. Many substrate nodes (sub*1*, sub*2* etc) will be defined for those divided layout regions, assuming minimal interactions between the regions. From those substrate nodes, equivalent resistive networks (in more elaborate study, RC networks) can be determined from vertical and horizontal

components of the distributed resistances connected to global/external grounds. Such a representation is shown in Figure 4.44. The resistances from the substrate nodes are defined as R_{subi}. Theoretically, their values may vary from zero (shorted to ground) to infinity (open). The RC networks and the capacitances to the sub*i* nodes are frequency-dependant components as well.

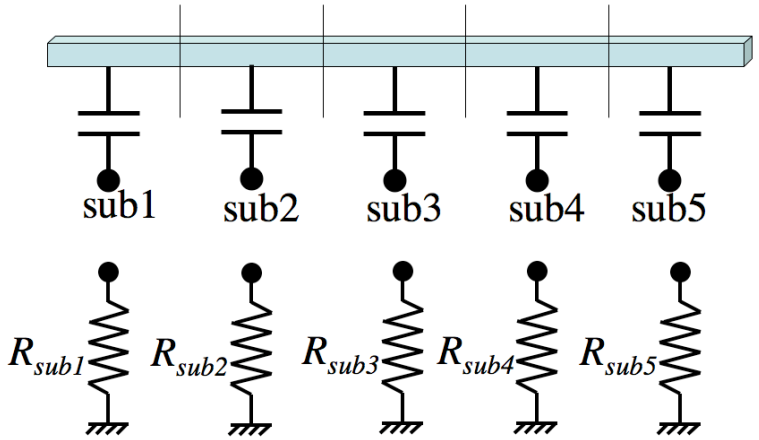


Figure 4.44. The substrate network approach for evaluation of the parasitic capacitance effects.

Now, if we look at different regions of layouts and divide it in large regions (say 100 x100 μm^2) the vertical substrate resistance component will be smaller than the distributed component. Hence, for simplicity, all the layout parasitics in that region can be connected to ground through that equivalent resistance. For smaller regions, the vertical component needs to be increased to have the same capacitive effects. If a line with 20 fF capacitance is cut into 20 pieces, and the substrate is modeled as an effective resistance of 50 ohm, then each 1 fF capacitance needs to be grounded by ~1 Kohm to maintain the same effect. Hence, the effect/impact should not change with the divisions. Also, the substrate resistances increase as we go further from the rings or substrate contacts.

In the following subsections, the substrate effects on CMOS and SiGe-HBT devices are studied in brief. In addition, the effects of substrate resistances on parasitic capacitances are analyzed using measured results from two parasitic structures.

4.5.1.1 Substrate parasitics on active devices and circuits

The substrate effects are more prominent in CMOS devices compared to HBT devices from device physics. For different commercially available processes, substrate effects are studied. For CMOS devices with 130 GHz f_T, the effects of substrate resistances on device impedances are shown in Figure 4.45. The device configuration chosen is cascode-connected devices with 40x1 μm width under 10 mA dc current consumption. The effects on circuit performance parameters, e.g., maximum available gain (for PA, LNA) and minimum noise figure (NF_{min} for LNA) are shown in Figure 4.46a and 4.46b respectively.

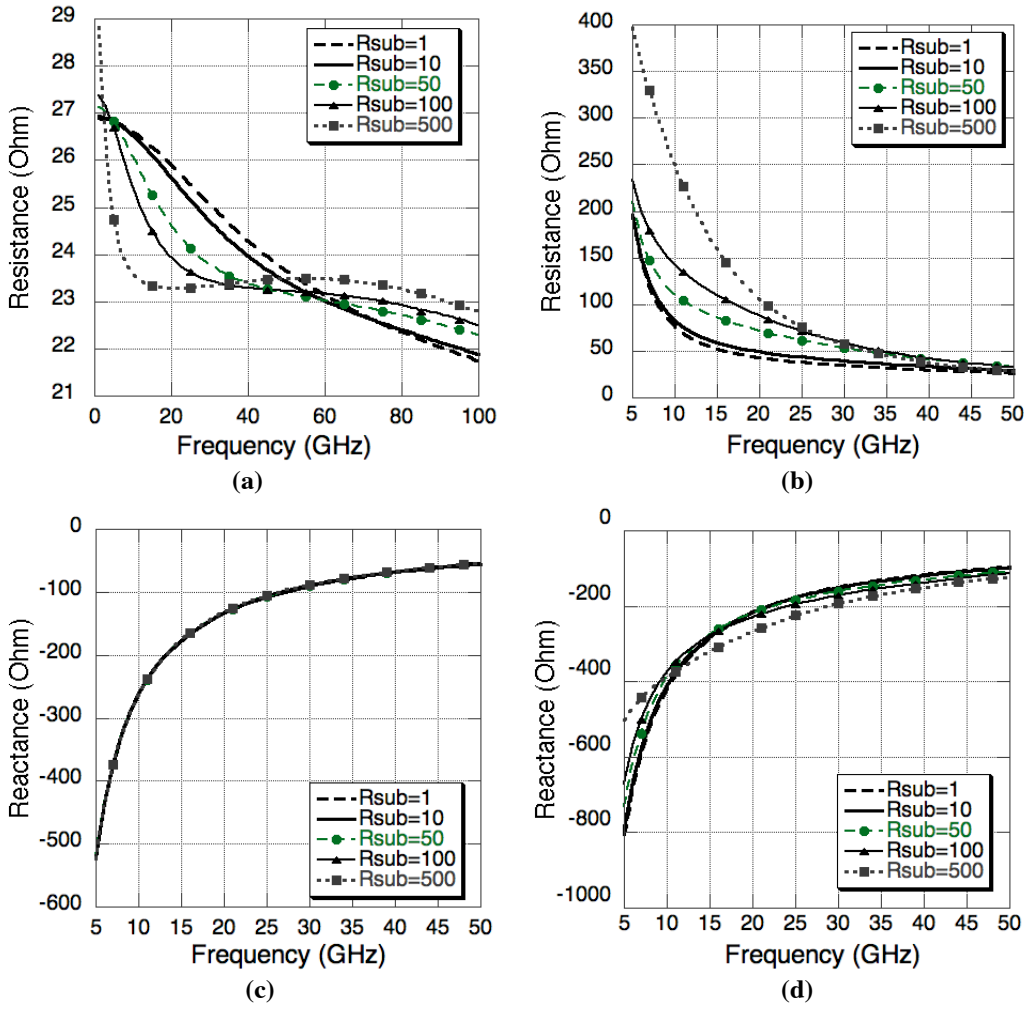
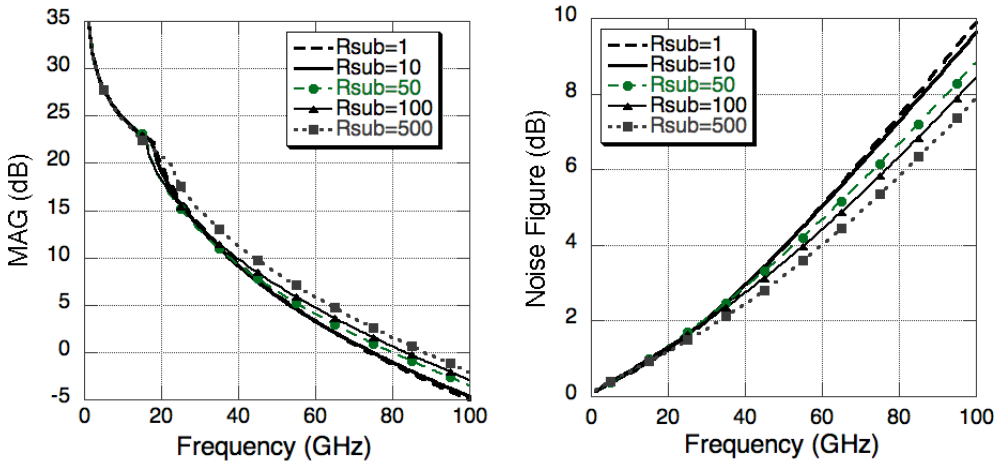


Figure 4.45. Looking impedances with varying substrate effective resistances.



(a) **(b)**

Figure 4.46. Circuit performance parameters.

For a chosen CMOS oscillator (shown in Figure 4.26), the effects of substrate resistance including and excluding them in device and layout interconnects are summarized in Table 4.5. Similarly, the effect on a 60 GHz CMOS LNA (with transmission line matching circuits) is shown in Figure 4.47. The effects are significant enough to demand an accurate modeling of substrate networks. Measurement-based device models can help to estimate the equivalent substrate network components.

Table 4.5. Effects on oscillation frequency for a CMOS oscillator

Substrate resistance	Substrate=ground for all the regions	Only active devices	Only in layout interconnects	In both
R=1	48.27GHz	48.27GHz	48.41 GHz	48.32GHz
R=10	48.27GHz	48.4GHz	48.61 GHz	48.62 GHz
R=50	48.27GHz	49.0GHz	48.73 GHz	48.76 GHz
R=100	48.27GHz	49.05GHz	48.67 GHz	48.77 GHz
R=500	48.27GHz	48.57GHz	48.62 GHz	48.7 GHz

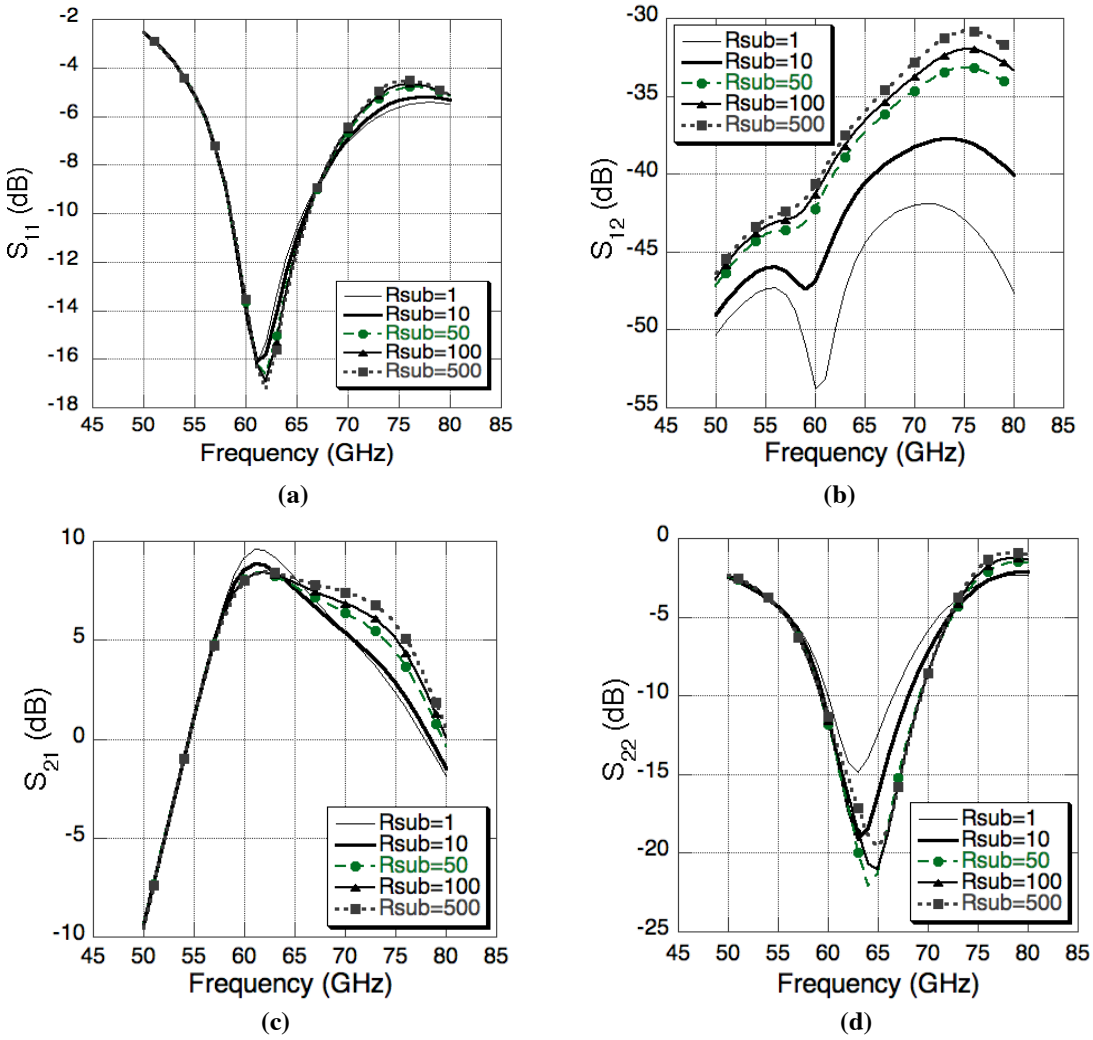
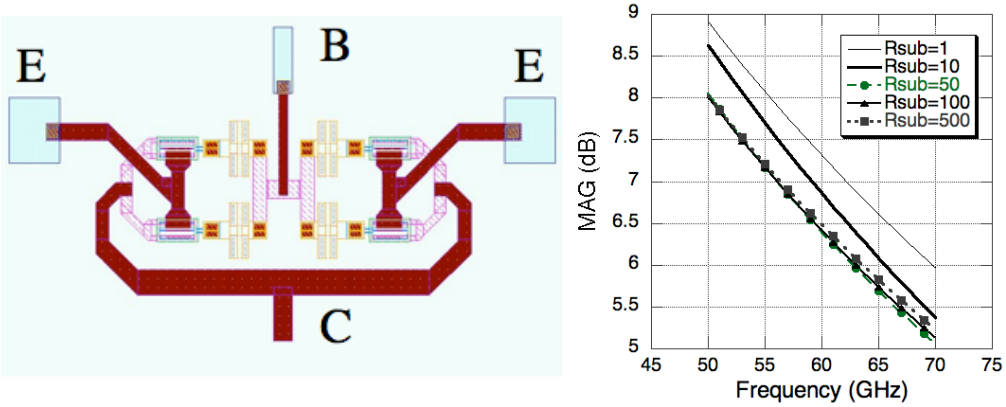


Figure 4.47. Looking impedances with varying substrate effective resistances.

For the SiGe HBT devices, the effects on device performances are insignificant but for bigger devices as used in power cells, the interconnect capacitances are affected by the substrate network. The variation of maximum available gain for the power cell shown in Figure 4.48a is reported in Figure 4.48b. The effects due to substrate resistances for a cross-coupled oscillator (described in section 4.4.2.1) are summarized in Table 4.6.



(a) (b)

Figure 4.48. Looking impedances with varying substrate effective resistances.

Table 4.6. Effects on oscillation frequency for a 30 GHz SiGe oscillator

Substrate resistance	Substrate=ground for all the regions	Only active devices	Only in layout interconnects	In both
R=1	31.75GHz	31.75GHz	31.75 GHz	31.75 GHz
R=10	31.75GHz	31.75GHz	31.75 GHz	31.75 GHz
R=50	31.75GHz	31.75GHz	31.70 GHz	31.70 GHz
R=100	31.75GHz	31.75GHz	31,64 GHz	31,64 GHz
R=500	31.75GHz	31.75GHz	31.57 GHz	31.57 GHz

4.5.1.2 Parasitic capacitance effects for different substrate resistances

Around active devices, substrate resistances are important as the device operation changes with their values. Far from active devices, the values of effective substrate resistances need to be considered mainly for to-substrate interconnect capacitances. In usual PEX tools, they are assumed to be ground but it depends on how many substrate contacts (TAPS) are included in the layouts. The substrate can be grounded for reliability and predictability. But sometimes they should not be grounded to avoid circuit failures from increased parasitic capacitance effects and to achieve a better performance.

Substrate resistance is mostly per region resistance. As described earlier, the number of substrate contacts in a specific region varies the substrate resistances for that layout region. Also, the effects of parasitic capacitances change with the number of substrate contacts. To prove this concept, two structures are fabricated in a state-of-the-art SiGe-BiCMOS process. The structures will be very similar for any other process. Figure 4.49 shows the structures. Structures 4.49a and 4.49b are different for the number of substrate contacts used. The structure on second metal layer from bottom with large number of substrate contacts is as shown in Figure 4.49a. Very few substrate contacts are used in the other structure shown in Figure 4.49b. The area of the structures and hence, the capacitance values are increased to reduce the effects of bond-pad.

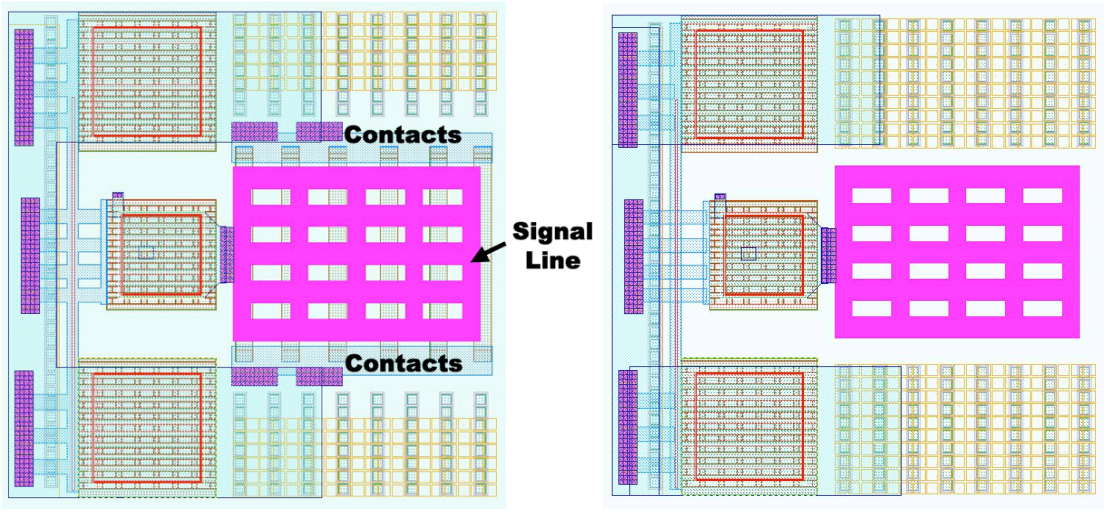


Figure 4.49. Layouts for parasitic structures.

Figure 4.50a and 4.50b shows the extracted capacitance and resistances from one-port S-parameter simulations for two structures. The difference in the substrate resistances with and without contacts changes the parasitic capacitance effects significantly. The resistances calculated from the contact resistances and verified using measurements at low frequencies for structures 4.49a and 4.49b are 5 ohm and 80 ohm respectively. The

capacitance values after de-embedding the effects of plate inductance (~75 pH) are shown in Figure 4.50c. In ADS platform, after including substrate model, the capacitances are compared as shown in Figure 4.50d (C1new = no substrate connections, C2new = substrate connections). The substrate equivalent network for the layout shown in Figure 4.49b is represented as 80-ohm resistance parallel with a 200-fF capacitance.

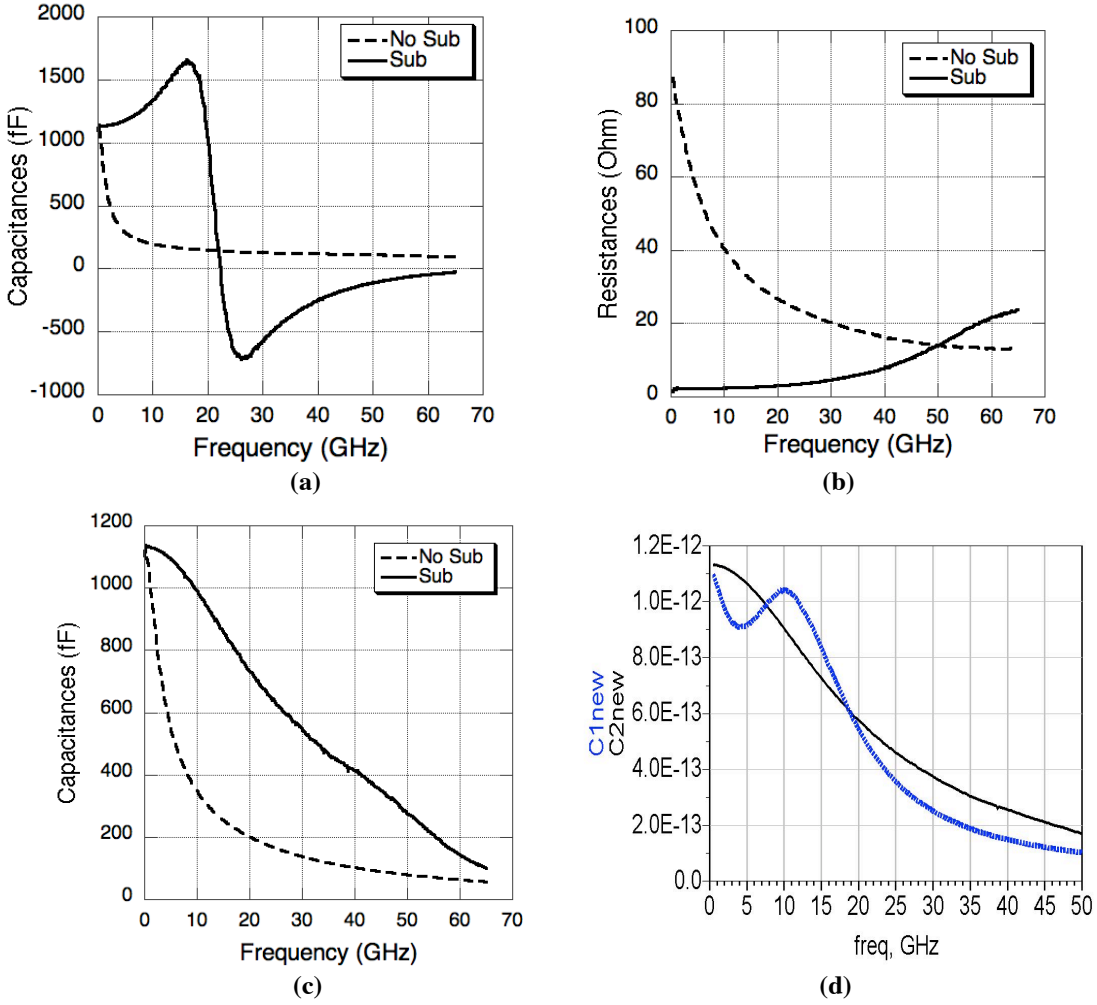


Figure 4.50. Capacitance and resistance comparison with varying substrate-grounding connections.

4.5.2 Process-related issues with examples

In this sub-section, the basic design and reliability issues in integrated circuits related to process variations are investigated. In addition, a design centering procedure and a circuit modeling technique using neural network models and genetic algorithms are

explained. The effects of process variations and the additional parasitics are demonstrated using Monte Carlo simulations for an MMW voltage-controlled oscillator (VCO) example.

The operation of devices, being close to their limits, brings reliability and design-optimization issues. Therefore, design centering has become one of the principal components of MMW IC design flow.

4.5.2.1 Design centering

The objective of design centering is to maximize the parametric yield of a circuit, i.e., to increase the number of fabricated circuits that satisfies a set of user-defined specifications [1.8]. In this work, a design centering methodology using neural network models and genetic algorithms is implemented. The basic flow [1.10] is shown in Figure 4.51. A Perceptron structure is assumed for the neural network models, developed from a simulation dataset. The input data points are chosen using LHS algorithm [3.6] in the range of the input values. Genetic algorithm is used to achieve convergence for the yield optimizations.

For 60 GHz systems, design centering has become very important to meet the stringent specifications of >2 Gbps data rate [1.2]. In addition, the process variations and modeling errors affect the circuit performances. At these frequencies, it is difficult to design over specifications. The variations using Monte Carlo simulations and different process corners are demonstrated using an example of MMW circuit in next sub-section. A detailed neuro-genetic design optimization including parasitics is proposed in section 5.2.

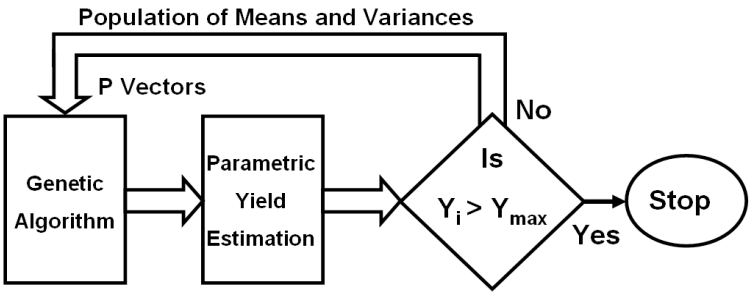


Figure 4.51. Neuro-genetic design centering.

4.5.2.2 Process variations on a MMW-circuit example

The effects of process variations on a millimeter-wave circuit are demonstrated using a 30 GHz VCO. The schematic of the cross-coupled [4.14] VCO, designed on a state-of-the-art SiGe-BiCMOS technology is shown in Figure 4.52.

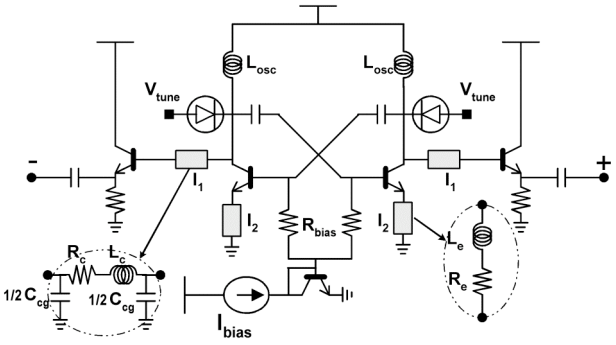


Figure 4.52. The schematic of the cross-coupled VCO used to study process variations.

The cross-coupled VCO (shown in Figure 4.52) is considered to investigate the process variations on a MMW circuit. Significant parasitic components are shown in the figure. Table 4.7 shows the variations of performance parameters for different process corners of transistors, capacitors and resistors. The center frequency varies from 28.27–29.89 GHz, power output varies from –0.45 to –4.5 dBm, and the second harmonic power varies from –16.2 to –24.2 dBm. This indicates the need for margins between required performances and designed performances.

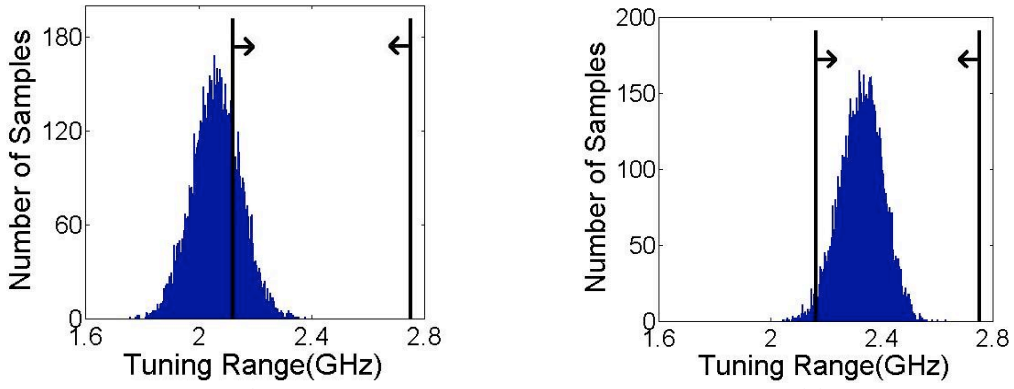
Table 4.7. The variation of circuit performances with different process corners

Components			Center Frequency (GHz)	Power@fundamental (dBm)	Power@2nd Harmonic (dBm)
NPN	CAP	RES			
Slow	Slow	Slow	28.42	-3.78	-22.40
Slow	Slow	Nom	28.36	-3.33	-21.00
Slow	Slow	Fast	28.27	-3.06	-19.44
Slow	Nom	Slow	28.77	-4.04	-23.12
Slow	Nom	Nom	28.72	-3.57	-21.56
Slow	Nom	Fast	28.63	-3.28	-19.88
Slow	Fast	Slow	29.20	-4.50	-24.29
Slow	Fast	Nom	29.15	-4.00	-22.5
Slow	Fast	Fast	29.07	-3.69	-20.60
Nom	Slow	Slow	29.03	-1.04	-19.98
Nom	Slow	Nom	28.89	-.927	-18.05
Nom	Slow	Fast	28.70	-.942	-16.17
Nom	Nom	Slow	29.41	-1.05	-20.10
Nom	Nom	Nom	29.28	-.936	-18.17
Nom	Nom	Fast	29.09	-.951	-16.29
Nom	Fast	Slow	29.89	-1.1	-20.1
Nom	Fast	Nom	29.77	-.977	-18.23
Nom	Fast	Fast	29.59	-.988	-16.39
Fast	Slow	Slow	29.19	-.459	-18.77
Fast	Slow	Nom	29.00	-.362	-16.51
Fast	Slow	Fast	28.75	-.365	-14.5
Fast	Nom	Slow	29.57	-.448	-19.02
Fast	Nom	Nom	29.39	-.351	-16.72
Fast	Nom	Fast	29.15	-.355	-14.68
Fast	Fast	Slow	30.06	-.448	-19.28
Fast	Fast	Nom	29.88	-.35	-16.95
Fast	Fast	Fast	29.65	-.356	-14.89

Not only process corners, but variations in design parameters (to achieve required performances) also need to be considered before optimizing the design. Now, let's consider Gaussian distributions for the emitter length, current bias as well as the varactor anode dimensions and check how the tuning range of a cross-coupled VCO gets distributed. For the analysis, VCO input parameters are shown in Table 4.8. The yield histograms with tuning range constraints (2.15-2.75 GHz) are shown in Figure 4.53 before and after design centering. To account for the parasitic variations, the design centering will be extremely critical (described in the next chapter).

Table 4.8. VCO input parameters

Input Parameter	Range for Mean		Dist. type	Standard Deviation
	Low	High		
Emitter Length (μm)	2	10	Normal	0.4
Ibias (mA)	2	10	Normal	0.4
Cvardim (μm)	10	30	Normal	1



(a) Before **(b) After**

Figure 4.53. Yield histograms of tuning range (2.15 –2.75 GHz for yield constraints) before and after design centering.

4.6 Summary

In this chapter, the transceiver blocks sensitive to interconnect parasitics are identified in different system implementation scenarios. The effects of parasitics around active devices are demonstrated using SiGe-HBT npn devices and CMOS devices with different feature sizes. A 90 nm NMOS device is used to verify the parasitic extraction with measurements for a wide frequency range. Layouts are differentiated into two types depending on their parasitic sensitivities. Later, estimation and optimization of parasitics are described for several MMW circuits, e.g., fixed frequency oscillators, VCOs, and frequency dividers. The effects of on-chip and off-chip parasitic inductances are shown for amplifiers at MMW frequencies. The role of substrate parasitics in device and circuit

performances is deciphered in this chapter. Also, the need for an effective design centering procedure for MMW circuits is demonstrated using VCO examples. Hence, it is evident that design and layout optimization are must for MMW circuits and systems. In the next chapter, the co-design and co-optimization procedure will be demonstrated for integrated transceivers consisting two or more circuit blocks that are described in this chapter.

Chapter 5

Co-design and Co-optimization with Parasitics for MMW ICs

5.1 Introduction

The design optimization is an extremely critical part of millimeter-wave circuit designs. Since, the ultimate goal is to implement these design topologies in an integrated environment as a system consisting of different blocks, the co-design and co-optimization of separate blocks, e.g., VCO, amplifier, mixer, and power amplifier, are very important to meet the stringent specifications of wireless standards. The design centering (described in subsection 4.5.2) is a necessity to reduce the number of design runs required to achieve the required performance as well as to increase the design yield. With the increasing complexity of the system architecture, the design yield needs to be maximized for wireless data transmission in millimeter-wave frequencies. The necessity to include the parasitic components in a design optimization procedure for the circuits as well as systems is demonstrated in Figure 5.1. Yield histograms are shown to identify the shifts of a performance parameter from process variations for an oscillator. The shifts from parasitics and the difference in the yield-histogram patterns before and after parasitic optimization clearly demonstrate the importance of design optimization including parasitics and the necessity of layout optimization.

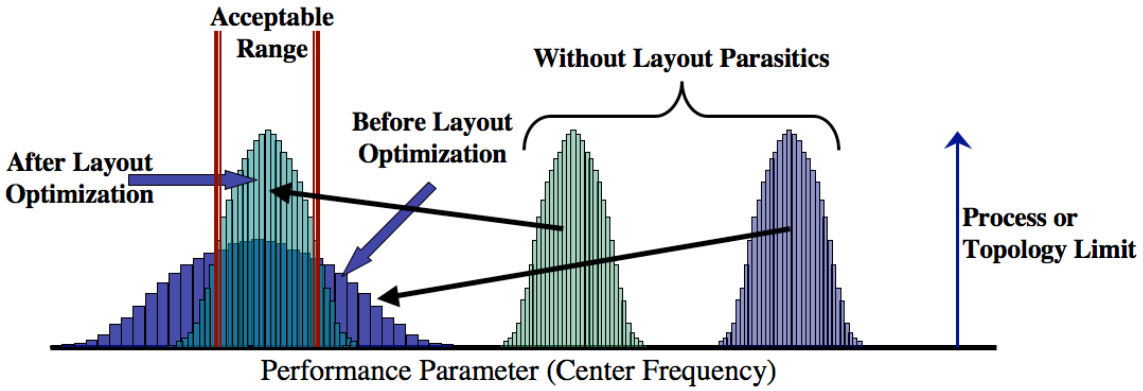


Figure 5.1. The design centering procedure including parasitics.

The two histograms shown on the right side are corresponding circuit behaviors without the parasitic components. The right most histogram shows a design without effective parasitic optimization. The performance parameter i.e. the center frequency of the oscillator/VCO is decreased by parasitics to the acceptable limit for both the cases. But in case of the parasitically optimized design, the percentage shift due to parasitics is less, and the histogram is less spread for reduced variations of parasitic effects from process variations. In addition, the parasitic components should be included in the design centering steps to reduce the spreading effect. The design yield will be affected by the spreading phenomenon. Also as evident from Figure 5.1, without an effective parasitic optimization, the design is closer to the process or technology limit and may not be able to meet other performance specifications.

In the next section, the systematic design optimization procedure is explained and demonstrated for a cross-coupled VCO using SiGe-HBT devices. In the third section, the layout optimization approaches are described in brief. Later, different transceiver blocks are co-designed including parasitic effects. An integrated up/down converter is implemented and used with LNA for a low-cost receiver at 60 GHz. Different blocks of a frequency synthesizer for a MMW system are described, and the complete layout is

studied. In the fifth section, the role of parasitics in certain system topologies is discussed in brief.

5.2 Systematic design optimization including layout parasitics

With appropriate sensitivity analyses and layout estimations, the number of variants can be reduced but still the prediction and characterization of the circuit parameters are the key components of a layout and design optimization approach for MMW ICs. The oscillator serves as a test-vehicle for the analysis since the oscillation frequency is extremely sensitive to the layout parasitics and the design parameters. Already, in section 3.3, the neural models are developed for parasitic elements, and later, in section 4.5.2, a neuro-genetic algorithm is introduced to optimize millimeter-wave circuits.

Moreover, to enhance the production yield, the design has to be centered properly so that the required performance is achieved even with process variations and modeling inaccuracies. Hence, it is very essential to identify the most sensitive design parameters. The identification of critical components and the corresponding design-centering procedure may vary from circuit to circuit, but the basic optimization algorithm remains the same. The proposed design optimization methodology is explained using initial simulation results from a 30 GHz VCO and later verified with measured results.

The most critical step for the yield optimization procedure is to identify the input design parameters and the layout parameters that may affect the yield [1.9]. The critical layout parasitics are identified from the sensitivity node analysis as well as the sensitivity analysis using the neural models. The complete design flow is shown in Figure 5.2. Firstly, a circuit topology is chosen according to the specifications. From initial simulations, the critical parameters need to be identified to develop neural models

representing the circuits. Genetic algorithm-based [5.1] or other systematic optimization methodology may be applied to optimize the design. The parasitics will be estimated from the initial layouts and accordingly, sensitivity analysis of design parameters. The estimated parasitics have to be used to redesign the circuit.

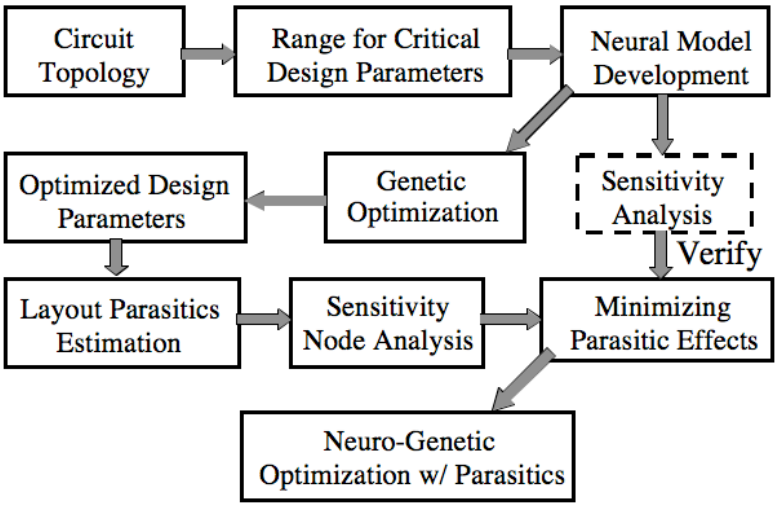


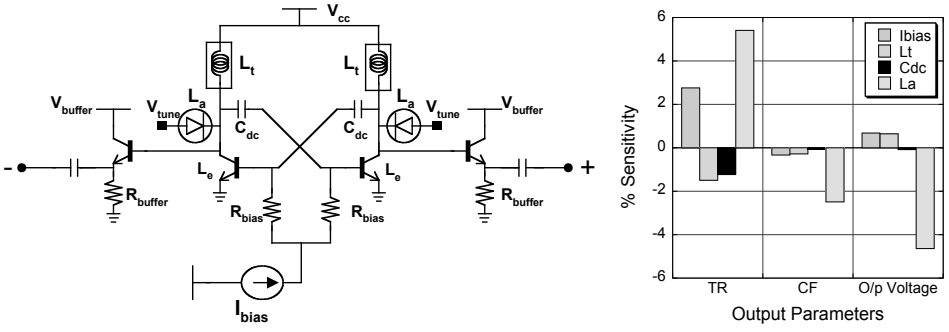
Figure 5.2. The design optimization procedure.

For the analysis, a 30GHz differential cross-coupled [4.14] VCO using npn SiGe HBTs is chosen as shown in Figure 5.3a. In the design-centering procedure, the output buffer is not taken into consideration for simplicity. However, the input parasitic capacitance of the buffer is included in the design. Also, a loss of 5 dB is assumed at the output of an emitter-follower buffer at 30 GHz.

The initial design parameters for the cross-coupled core are the emitter length (L), the bias current (I_{bias}), the power supply (V_{cc}), the varactor dimensions (anode width W_a and length L_a), the dc coupling capacitor (C_{dc}), and the length of the inductive line on the top metal layer (L_t). High-Q MIM capacitors are used whose reliability constraints narrow down the usable range of capacitors. The ranges for the input parameters are determined for the given tuning range of the VCO from the initial simulations and theoretical analysis. The supply voltage, Vcc (1.2 V), and the emitter length of the SiGe devices (5

μm) are chosen considering the required trans-conductance and the power handling capacity along with the buffer specifications. The anode width is fixed and the anode length (L_a) is varied, which simplifies the design centering procedure. Thus, the four input parameters are chosen as I_{bias}, L_t, C_{dc}, and L_a. The output parameters chosen are the tuning range (TR), the center frequency (CF), and the output voltage amplitude.

After the choice of the significant input and output parameters, neural network models based on the Perceptron algorithm [2.1] are developed for the maximum and minimum oscillation frequency as well as the output voltage amplitude. Accordingly, the sensitivity analysis (shown in Figure 5.3b) is performed using the models. At 30 GHz, the effects of parasitics may change the output parameters by as much as 30% (39.2 GHz to 30 GHz). That signifies the problem in design centering as represented in Figure 5.1. Therefore, the optimized parasitic matrix has to be included in the design.

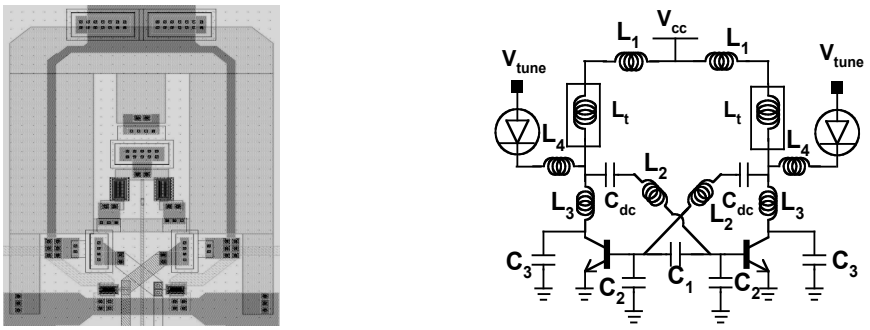


(a) **(b)**

Figure 5.3. (a) Schematic of the cross-coupled topology; (b) the sensitivity analysis for the design parameters.

From the sensitivity bar diagrams in Figure 5.3b, it is evident that the anode length of the varactor is a very important design parameter that dictates the tuning range as well as the output voltage amplitude. Also, the inductance L_t is critical to decide the oscillation frequency. The effect of C_{dc} is comparatively less than the other components. From these sensitivity plots, the design parameters are selected according to the required

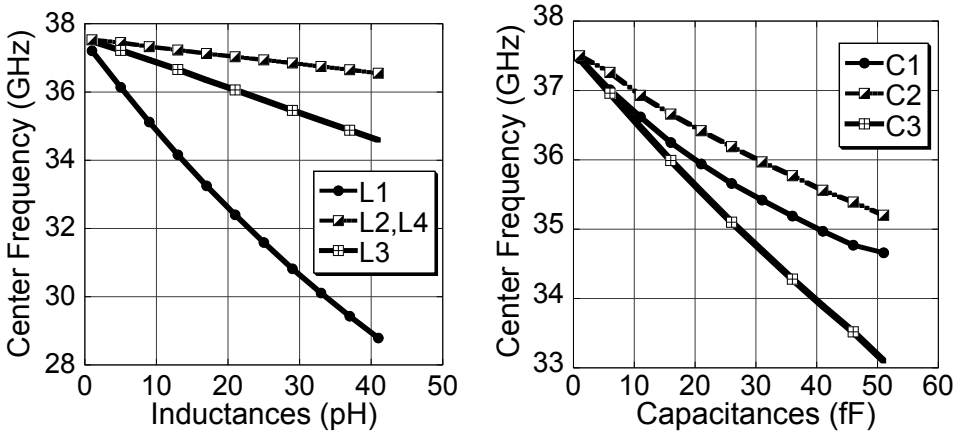
specifications. For example, the TR and CF values without parasitics have to be much higher than the specified values. As the next step, the sensitivity node analysis for the parasitic inductances and capacitances should be performed for the layout and parasitic matrix as shown in Figure 5.4a and Figure 5.4b respectively.



(a) (b)

Figure 5.4. (a) The layout; (b) the parasitic component matrix for the cross-coupled core.

Figure 5.5 plots the effect of the parasitic inductances and capacitances on the oscillation frequency. It is interesting to note that the inductors L_1, L_3 and the capacitor C_3 turn out to be the most critical parasitic components, and that is also verified from the sensitivity analysis in Figure 5.3b.



(a) Inductive effects **(b) Capacitive effects**

Figure 5.5. Effects of parasitic inductance and capacitance components.

The parasitic components are estimated using neural network models developed from EM simulations. The ranges of the input parameters can be reduced using the sensitivity analysis. These ranges are used for developing the second-generation neural models for

the final design centering including the parasitic network. Again, the genetic algorithm is applied to choose the set of means and variance vectors for the active circuits. During genetic manipulations, the samples with higher yield (calculated using Monte-Carlo simulations) are assigned greater "fitness" values, leading to a higher probability of survival in the new population set. The process is continued iteratively until a suitable design-center is achieved [5.2]. The variations of the input parameters are assumed to be random/normal depending on its type. The results of the optimization using the neuro-genetic algorithm are summarized in Table 5.1.

Table 5.1. Design centering of VCO

Input Parameters				
	Initial Value (Yield=4%)		Final Value (Yield=86%)	
	Mean	Std	Mean	Std
I_{bias}(μA)	54.1	0	47.8	0
L_t (μm)	141.5	6	144	6
C_{DC} (fF)	179.4	10	171.7	10
L_a (μm)	9.1	0.4	8.0	0.4
Output Parameters				
Yield Constraints	Initial Value		Final Value	
	Mean	Std	Mean	Std
Tuning Range (2.15-2.75 GHz)	1.99	0.16	2.41	0.14
Center Frequency (29-31 GHz)	29.0	0.53	29.9	0.64
Output Voltage Amplitude (> 350 mV)	497	9.00	508	6.10

From the results of the yield, it can be seen that the yield has been increased upto 86% within 200 iterations of the algorithm for all input parameters with normal distributions. In the case of random distributions, the yield is increased from 30% to 91%. As evident from the mean values, the effect of the varactor dimension is the most

prominent among the yield improvement results that is coherent with the sensitivity analysis.

With the understanding of sensitivity analysis and the neuro-genetic optimization procedure, 30 GHz differential cross-coupled VCOs are designed, optimized, and fabricated using a 0.15 μm SiGe-BiCMOS process. Measurements show excellent match with the final optimized results. A center frequency of 30.5 GHz with a tuning range of 2.3 GHz was achieved. The maximum power measured at the buffer output is around -10 dBm at 29.54 GHz. The die photo of the fabricated IC and the measured spectrum at 29.6 GHz are shown in Figure 5.6(a) and Figure 5.6(b) respectively. The best phase noise is around -94 dBc/Hz at 1 MHz offset as shown in Figure 5.6(c).

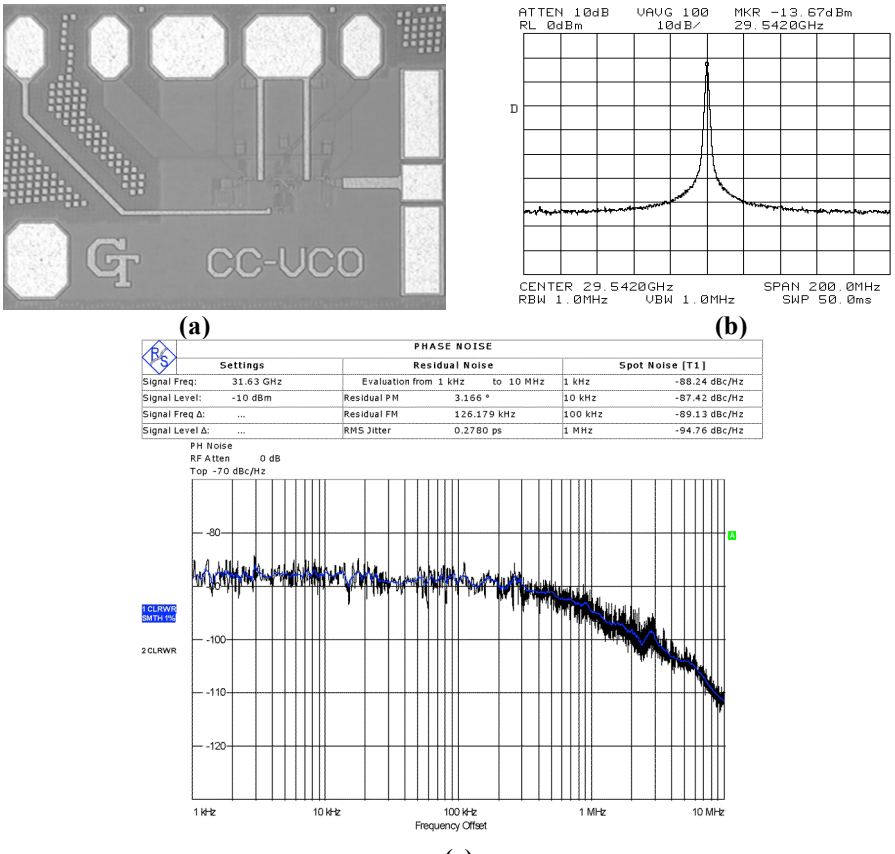
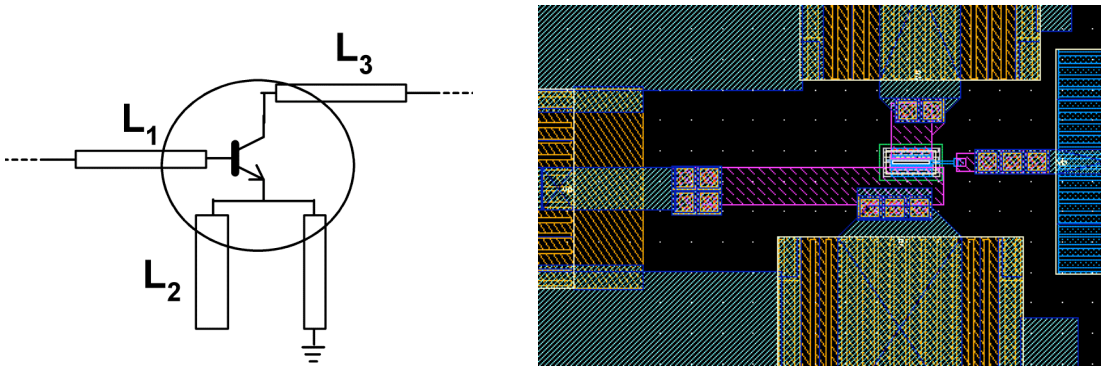


Figure 5.6. (a) Chip die photo, (b) measured output power and (c) measured phase noise for the 30 GHz cross-coupled VCO.

5.3 Layout optimization of MMW ICs

The layout optimization for parasitics is an important step in the designs of MMW ICs. Minimization of all the parasitic components is not always possible, and it is not essential too. However, the identification of significant interconnect-components and optimization of the dimensions according to circuit performances is very important. In an integrated system approach, the large numbers of transmission lines as well as RF- and DC-pad connections make the layout optimization [5.3] very difficult.

Most of the parasitics are unavoidable in order to satisfy the design rules in a multi-layer process. The transmission lines are generally realized in the top metal layers and used for matching/tuning the circuits. Active devices, being connected to lower metal levels, require 3D interconnects. The nodes/signal paths need to be determined where the presence of parasitics will affect the most. Figure 5.7 shows the connection of active devices to corresponding microstrip/CPW lines for a 60 GHz oscillator in Colpitts configuration (described in 4.4.1.1).



(a) Device connections **(b) Layout connections**

Figure 5.7. The device and layout connections for the 60 GHz oscillator.

The selection of metal layers for interconnects in RF/MMW circuit layouts demands a sensitivity analysis of designs for the node capacitances/inductances. In general, top

metal layers are used for high current carrying capacity, less 'to-ground' 1-port capacitances. On the other hand, thin metal layers (close to ground plane) may have less inductive effects, but the parasitic capacitances and resistances may prove to be critical for the circuit design.

The resistances and inductances are also significant for the via-structures in the layout. The electrical characteristics of the via-cells need to be estimated using EM solvers. However, the use of parallel via blocks can reduce their effects on circuit performances. Considering all the external parasitics for active devices, the connections between P-Cells (already characterized standard layouts), and the transmission line modes in embedded conditions, the floor-planning need to be revised manually or automatically to ensure required performances.

A set of layout guidelines for MMW ICs are developed considering CMOS and SiGe-BiCMOS processes, and different layout optimization issues are investigated as follows:

(i) Inter-block connections: When two or more blocks are integrated, the parasitic issues rise in the interface where the outputs of one block are fed to the other block. In certain cases, this interface is simplified using merged transmission-line matching structures. One such example is demonstrated in Figure 5.8. In this figure, an integrated layout for the switched and power amplifiers is shown considering an ASK implementation (Figure 4.14). The switched amplifier is used to modulate as well as amplify the carrier signal generated by the oscillator.

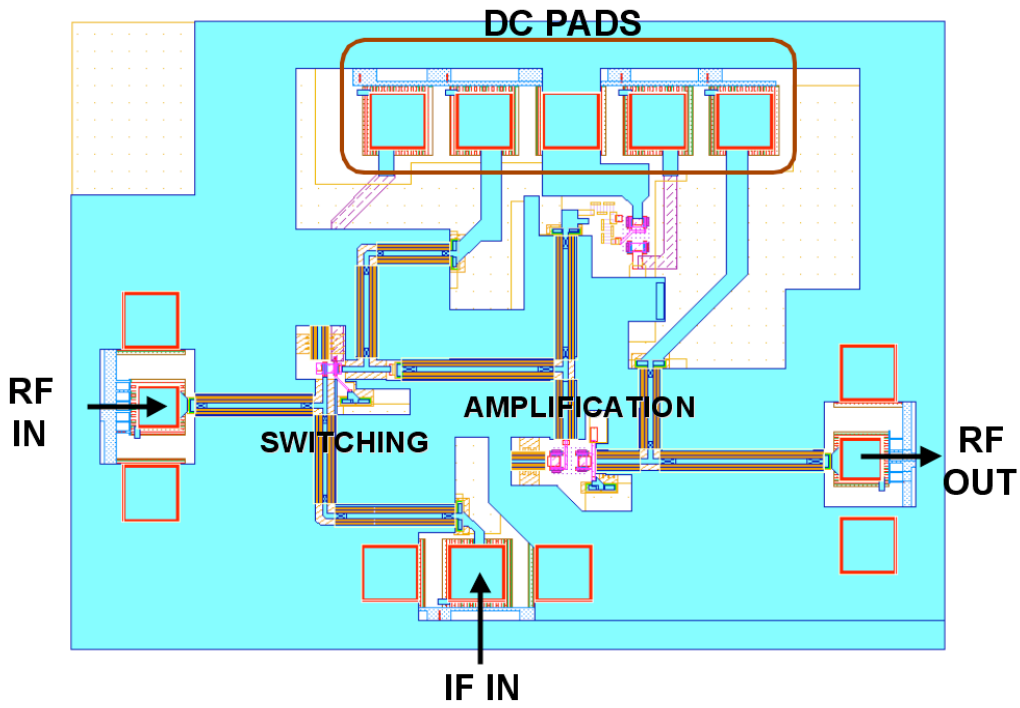


Figure 5.8. The layout of the integrated amplifier.

In the above layout, the transmission-line matching elements between switched amplifier and power amplifier blocks effectively minimize the parasitic effects in the inter-block connections. But the scenario will not be same while realizing the connections of a Gilbert-cell mixer [4.2] or a VCO to divider connections (described later). The problem arises while maintaining the form factors for layouts and the symmetry of connections.

(ii) Vdd line resistance: The sheet resistances of vdd lines are critical while implementing a system with three or more blocks. The pad connections cannot be realized close to the vdd nodes for all the separate circuits. Hence, there are long vdd connections for some of the nodes. Say, for example, the power supply connections for the mixer and the amplifier for VCO are both fed by 1.8 Volts. But, the vdd pad is placed closer to the mixer and hence, there is a routing resistance of 5 ohm to the power supply

connection of the amplifier. If the amplifier consumes 20 mA, there is a voltage drop of 100 mV. This will be even more critical for cross-coupled structures where the gate and drain connections are shorted. In that case, a 100 mV of decrease is equivalent to a significant change in the performance. If all the blocks are designed with the same power supply, in the implementation, they will receive different voltages. In addition, for differential circuits, these power line drops will create imbalances.

Consider a 2.5 mm by 2.5 mm chip with a 3 mm power line routing in a CMOS process with 100 mΩ sheet resistance with maximum possible line width as 10 μm. The resistance will be more than 3 ohm. If more than one block is connected to the same supply resulting more than 100 mA of current, there is a significant drop of 300 mV.

One possible solution is to use power supply pads close to the nodes in different circuits but in a system-level implementation that is not effective. A better solution is to use metal stacks i.e. to route more than one metal layers on top of other and hence, putting more resistances in parallel. Also, using parallel paths for connections to the pad will reduce the resistance. For the above-mentioned example, using 3 parallel paths and 3 metal stacks for each, the 3-ohm resistance can be reduced to less than 0.5 ohm.

(iii) Routing of dc lines: With increasing number of blocks, the pad connections to the power supply lines need to be routed to minimize resistance and at the same time, not to affect the RF blocks. Since a dc line will act like a ground for transmission lines, it is important not to over lap them. In such layout scenarios, a roundabout routing solution can solve the problem but, at the same time, it increases the routing resistance. An effective solution is to use the dc-blocking caps for routing dc lines below them given it does not affect the circuit performance.

(iv) Ground-continuity and ground resistance: The ground resistance is extremely critical for RF performances of the transistor as well as the working principle of transmission lines. The ground should be continuous all around the chip to reduce the ground resistance. For a well-distributed ground, ground pads should be placed all around the chips and preferably, closer to the power hungry blocks.

(v) DC-coupling capacitors: As described in subsection 4.4.3, the DC–coupling capacitors should be put as many as possible in power/vdd lines to avoid any DC oscillations.

(vi) Substrate connections: The substrate resistance should be low in CMOS processes for better transistor performances. For SiGe-BiCMOS process, they may not be that important from SiGe-transistor-performance point of view, but to characterize the effects of parasitic capacitance, they should be either low or very high. Also, isolation of substrate is important to reduce substrate coupling when it is not desired.

(vii) Feeding RF/IF through pads: The RF and IF connections to pads should be well characterized or of small electrical length. Thus, the blocks with external connections need to be placed close to the pads, and other blocks need to be floor-planned accordingly.

(viii) Compactness and performance trade-off: To reduce the production cost, the layout needs to be as compact as possible. To make it compact, bends have to be used in transmission lines without RF lines crossing each other though it is difficult to avoid side-coupling completely. To make it more compact, the power-line width may need to be reduced closer to the separate circuit blocks thus increasing the power line resistance. The reduction of RF signal line dimensions and the use of thin metal layers for connections

may lead to unwanted loss in RF path. Also, in a compact layout, wide grounding is not possible and hence, the performance degradation from ground resistance.

5.4 Co-design including parasitics

In the last chapter, the effects of parasitics in the design of separate blocks are demonstrated. In this section, the co-design of different blocks including parasitics is studied in detail. The parasitic-sensitive oscillator layouts are integrated with different transmission-line-based layouts. The co-design and co-optimization solutions are demonstrated using system blocks, e.g., VCO-amplifier, up/down converter, and VCO-PLL.

5.4.1 Design and layout of VCO-amplifiers

In this subsection, a cross-coupled differential VCO and a push-push VCO with single-ended amplifiers are considered in two different processes. Differential amplifier co-design with a differential VCO is considered in the next subsection as a block of integrated VCO-PLL.

5.4.1.1 Cross-coupled SiGe-HBT VCO with amplifier

The VCO is implemented using a cross-coupled topology with emitter-follower buffers as described in sub-section 4.4.2.1. The schematic of the VCO-amplifier is shown in Figure 5.9. The most important parameter for VCO-amplifier co-design is to achieve the output power with an acceptable phase noise. The up or down converter mixers at 60 GHz usually require higher LO power to achieve decent conversion characteristics. Thus, the optimization of VCOs including parasitics is done with stress on the output power of the VCO and phase noise. The frequency shift due to parasitics is reduced from 15% to

6% with parasitic estimation and optimization. The capacitive effects are minimized to reduce the effects due to substrate resistance variations.

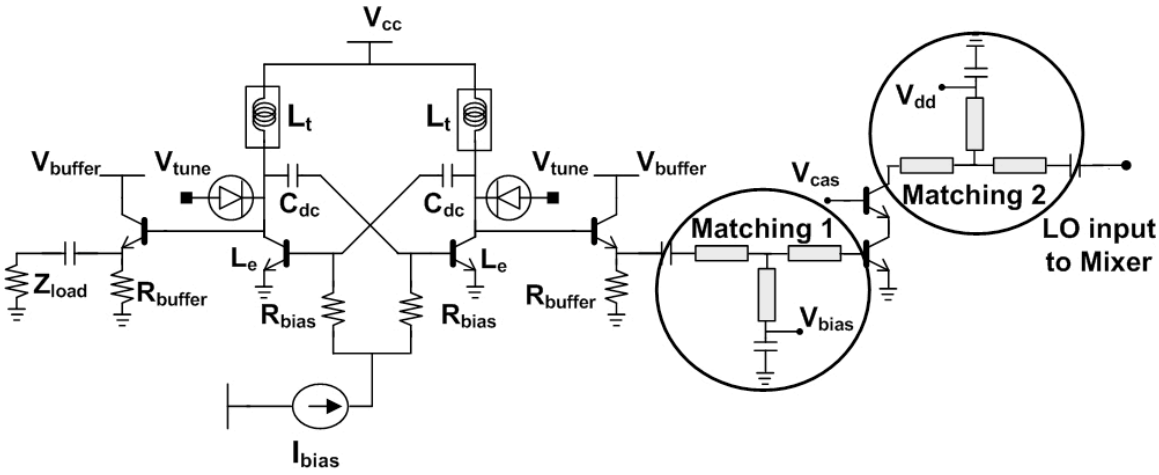
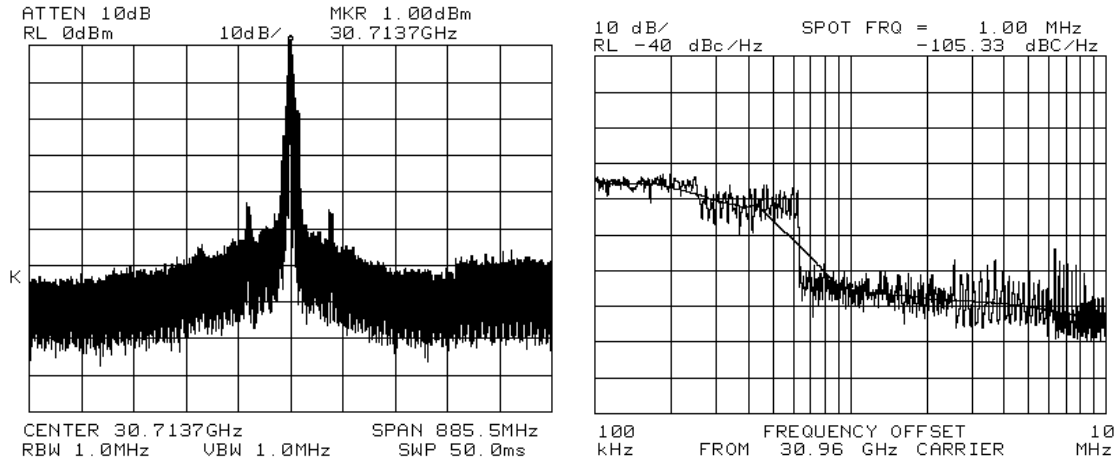


Figure 5.9. The schematic of VCO-amplifier.

The matching networks are designed to act like a buffer at the input and to match 50 ohm to the output. The mixer input impedance is assumed to be matched at 50 ohm. The matching networks are realized using conductor-backed co-planner waveguide (CB-CPW) lines with the thicker top metal as signal line. For the isolation provided by the emitter follower buffer, the oscillation frequency is not sensitive to the amplifier matching networks. The amplifier output is matched to the mixer LO-input impedances for maximum gain of the amplifier. A test structure of the VCO-amplifier is implemented in a 180 nm SiGe-BiCMOS process. The measured results are shown in Figure 5.10. A measured output power of +5.5 dBm is demonstrated for only 40 mW of dc power consumption. The output power level is achieved using 18x0.2 μm^2 devices. Since the oscillator is loaded with optimum higher impedance values instead of 50-ohm loads (as, in the case of VCO test structures), the best phase noise is better than that of separate VCO structure, and it is reported as -105 dBc/Hz at 1 MHz offset in Figure 5.10b. The die area is 1.4 x 0.9 mm^2.



(a) **(b)**

Figure 5.10. (a) The spectrum (with a 4.5dB loss) and (b) the phase noise characteristics of the VCO-amplifier.

5.4.1.2 Push-push CMOS VCO with amplifier

The buffer-amplifier design is more critical in CMOS processes for the reduced power handling capacity and lower maximum-available gain (MAG) compared to SiGe processes of the same device feature size. In a 90 nm CMOS process, a push-push VCO is integrated with a single stage cascode amplifier to feed up/down conversion mixer. The push-push VCO is designed using the parasitic benchmarking procedure as described in sections 3.4 and 4.4.2.2. Though the push-push output is not terminated at 50-ohm impedance, the same benchmarking set up can be used for the isolation of source follower buffers. The output impedance is chosen to maximize the output power. The amplifier is designed using transmission line models. Since, there are more than one matching networks to achieve the same power level, the layout constraints on the integrated VCO-amplifier-mixer is used to determine the final transmission line lengths. The amplifier DC current consumption is varied to change the input LO power level as required for receiver and transmitter. The output matching circuits are different for receiver down-conversion and transmitter up-conversion mixers. The VCO-amplifier

integrated layout is shown in Figure 5.11. It is a combination of two different types of layouts. The cross-coupled core is more dependent on parasitics, and the buffer/amplifier section is more transmission-line-based. The VCO-amplifier is integrated with a mixer-PA integration, and it has an output power of 0 dBm for 50-ohm load. The total power consumption is 35 mW for a tuning range of 5 GHz centered at 52 GHz.

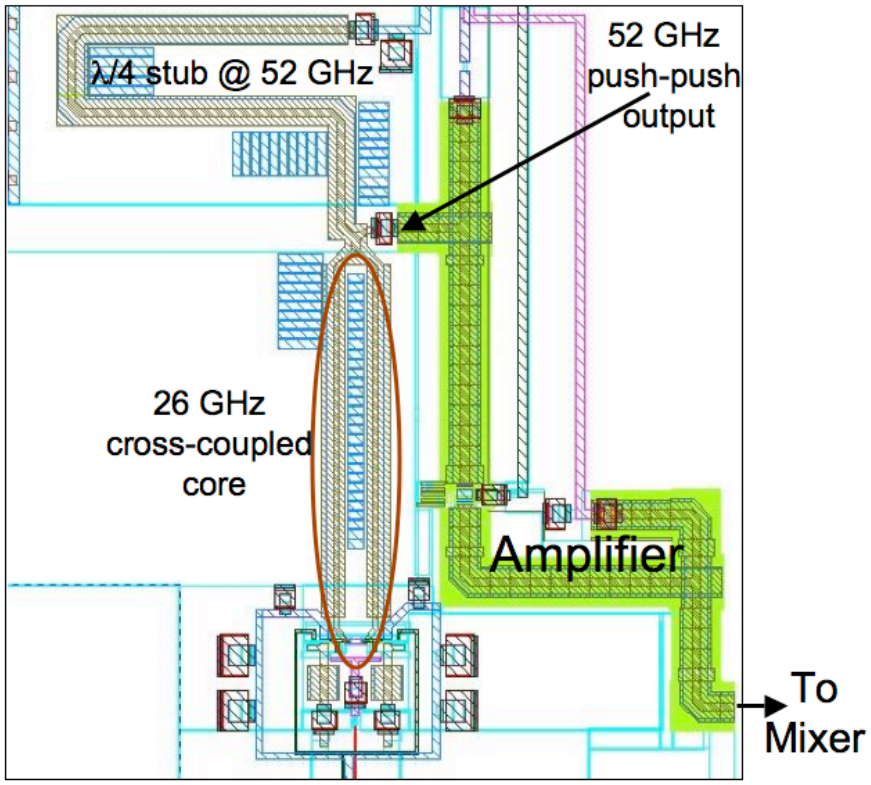


Figure 5.11. The schematic of the CMOS VCO-amplifier.

5.4.2 Design and layout of an integrated up/down converter

In this subsection, the design of an integrated up/down converter is described and in the next subsection, the design is modified to include in a low-cost receiver at 60 GHz. The VCO-amplifier design methodology is applied with desired modifications of output matching for the amplifier to reduce loss in the matching elements.

The system specifications for low-cost 60 GHz front-ends in silicon-based technologies demand a low-power, wideband, and compact up/down converters. Silicon-based technologies always have an edge over the III-V semiconductors in terms of the cost and integration. The introduction of silicon-germanium (SiGe) hetero-junction bipolar transistors (HBT) [5.4] already narrowed the performance shortcomings of the silicon-based technologies. Hence, it is suitable for 60 GHz system integration [1.1, 2.12].

The passive sub-harmonic mixing topology is useful for a compact transceiver module as it can provide the up/down conversion functions together. It is also shown to have a significantly larger bandwidth than other mixing topologies [5.5, 5.6]. One such system architecture is shown in Figure 5.12, with the portion in the dotted box being implemented in this particular work.

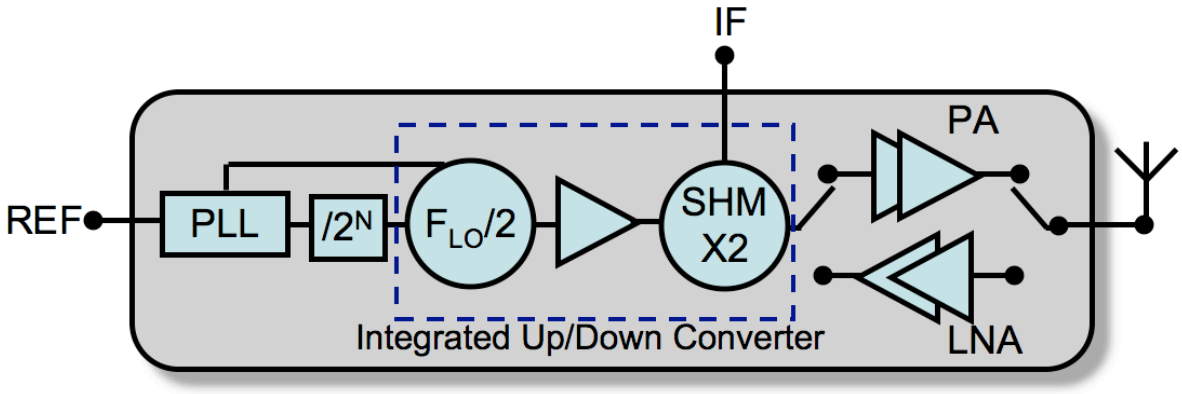


Figure 5.12. Low-power low-cost 60GHz system architecture.

This system requires a PLL to synchronize the 30 GHz VCO. SiGe technology is capable of providing the gain for LNA [4.11] and PA [5.7] to compensate for the conversion loss of the sub-harmonic mixing. The mixing scheme, if required, can be modified to work with direct-conversion as well super-heterodyne architectures. Although in this particular implementation, a direct-conversion architecture is

implemented to minimize the complexity, die area and more significantly, the power consumption. In the next subsection the integrated VCO-mixer will be modified to apply the same design methodology in a super-heterodyne architecture.

The design procedure is summarized in Figure 5.13. For the integrated up/down converter, shown in Figure 5.12, the targeted power level for 30 GHz VCO output is around -5 dBm, and the amplifier is used to increase that level to +5 dBm required for sub harmonic mixer. The VCO-amplifier co-design is very critical for tuning characteristics, power output and noise performance as described 5.4.1.1.

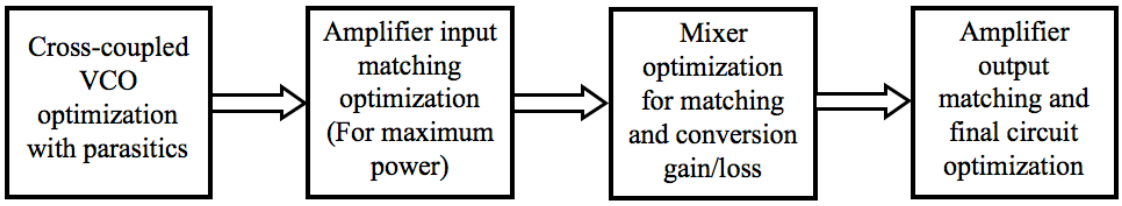


Figure 5.13. Design flow of 60GHz low-cost up/down converter.

An anti-parallel-diode-pair-based 2X sub-harmonic mixer is implemented. The mixer block can be used for both up and down conversion. All the transmission lines are realized in a CB-CPW mode in order to minimize the radiation losses as compared to the micro-strip implementation. A base-collector-shorted npn HBT is used as a diode [5.5]. A 200 fF MIM capacitor replaces the usual RF $\lambda/4$ coupled line to minimize the die area. The inductive parasitics for the MIM capacitor is included in the design. However, the loss of the capacitor as well as the reduced isolation between RF and IF ports increase the conversion loss. Figure 5.14 shows the schematic of the integrated VCO-mixer.

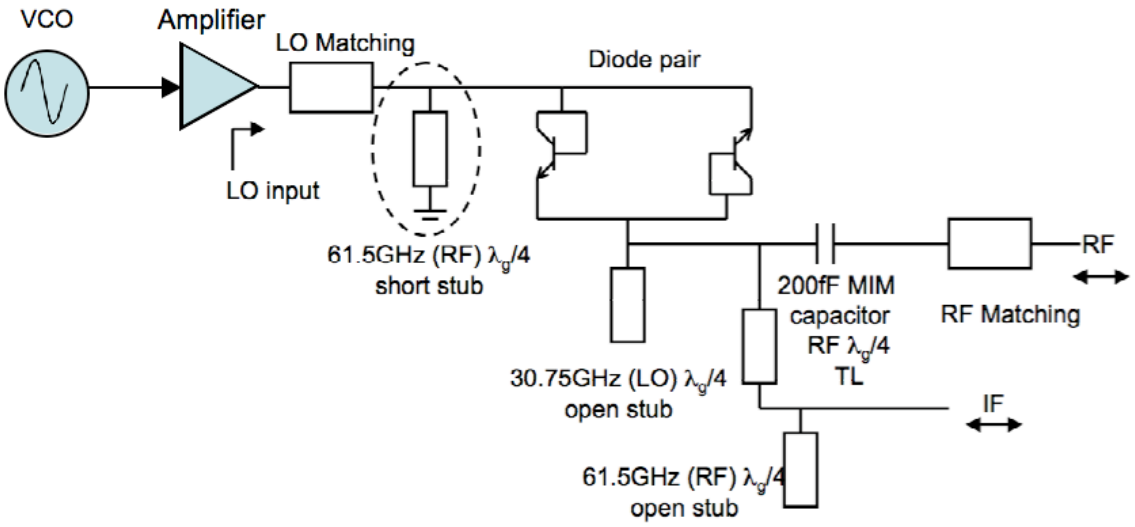


Figure 5.14. The schematic of the integrated up/down converter.

The VCO-mixer is measured using on-wafer testbed with Anritsu MG3696B (RF) source and Agilent 11474V spectrum analyzer. The noise figure is measured using Agilent N8972A. The conversion loss characteristics with RF frequencies (compared with simulation results) are plotted in Figure 5.15a for LO frequency of 30.75 GHz. The slight mismatch (~2 dB) of measured and simulated results can be attributed to additional transmission line losses and reduced LO power. The conversion loss for up conversion is shown in Figure 5.15b. The measured 3-dB RF bandwidth is more than 9 GHz in both the modes. The integrated up/down converter has 11 dB and 12 dB conversion losses in up and down conversion modes respectively. The spectrums for down and up conversion are shown in Figure 5.15c and 5.15d respectively. The measured results are summarized in Table 5.2. The die photo is shown in Figure 5.16. The die area of the up/down converter is only 1.4 x 1.2 mm^2.

For amplifiers or mixers the matching circuits are designed using models available in the design kit. The device parasitics are less for the use of single-finger and smaller transistor sizes compared to CMOS devices for similar power requirements. The

parasitics effects are prominent in the connections between transistors and transmission lines because they affect the input looking impedances for narrow band matching networks. These effects are more significant in the output matching networks for cascode-connected devices. The neural models based on EM tools are used in all those parasitic possibilities. The ground resistance is decreased to have better performances from the transistors and transmission lines.

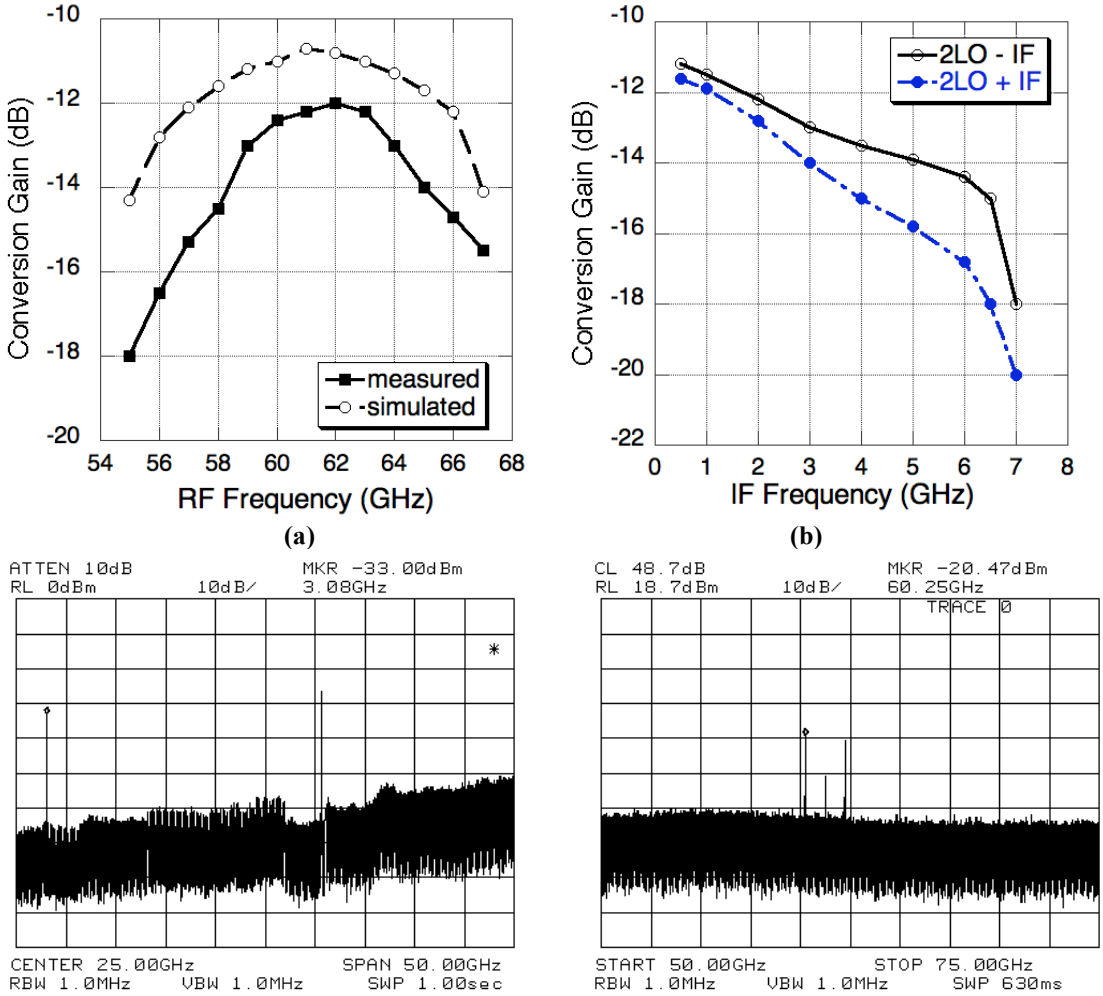


Figure 5.15. (a) & (b)The conversion characteristics and (c)& (d) the output spectrum for the integrated up/down converter.

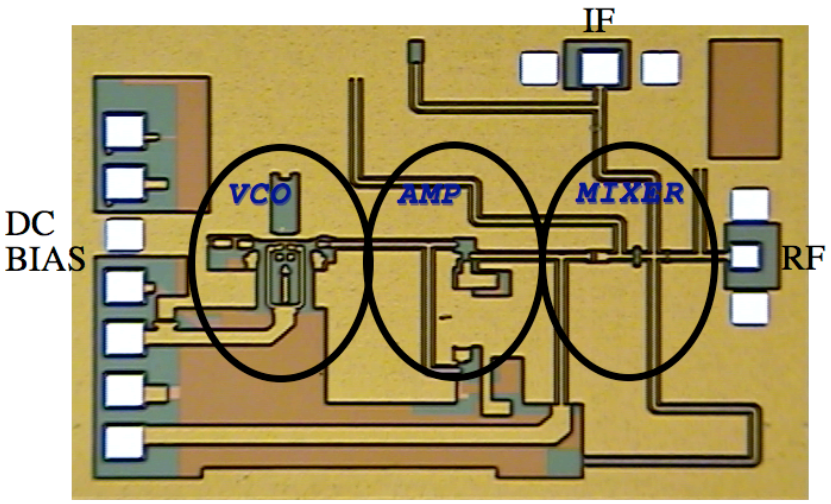


Figure 5.16. The die photo of the integrated up/down converter.

Table 5.2. Performance summary of the up/down converter

Conversion loss	12 dB @1 GHz IF for down conversion 11 dB @1 GHz IF for up conversion
RF matching	<-10 dB for 59.5-63.5GHz
3-dB RF bandwidth	>9 GHz
Noise figure	15±2 dB@1 GHz IF
Input P1 dB	-2dBm @1 GHz IF in up conversion
DC power consumption	< 40 mW
LO leakage	-26 dBm @30.75 GHz

5.4.3 Implementation of a receiver at 60 GHz

A sub-harmonic heterodyne receiver front-end is developed in 0.18 μm SiGe BiCMOS process. A three-stage LNA [4.11] is integrated with a 2X passive sub-harmonic [5.5] mixer for the heterodyne front-end with on-chip LO generation block. Figure 5.17a shows the block diagram of the receiver front-end. Figure 5.17b shows the die photograph of the integrated receiver front-end using 0.18 μm SiGe BiCMOS

process. The die area of the integrated LNA-mixer-VCO chip is approximately 3.5 mm × 1.2 mm.

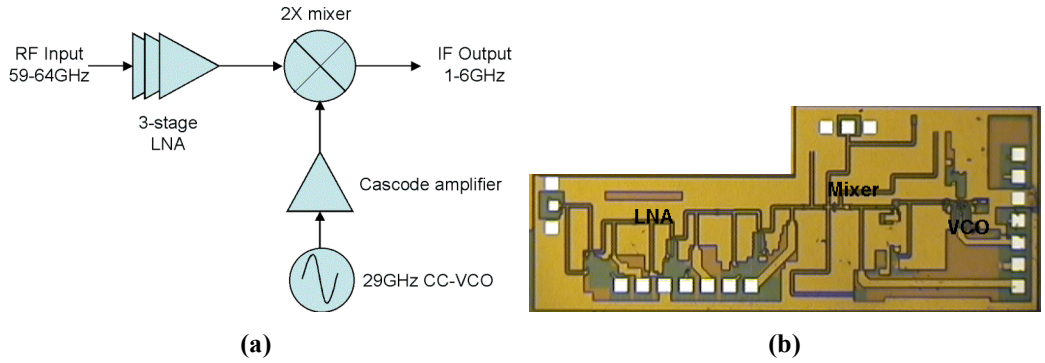
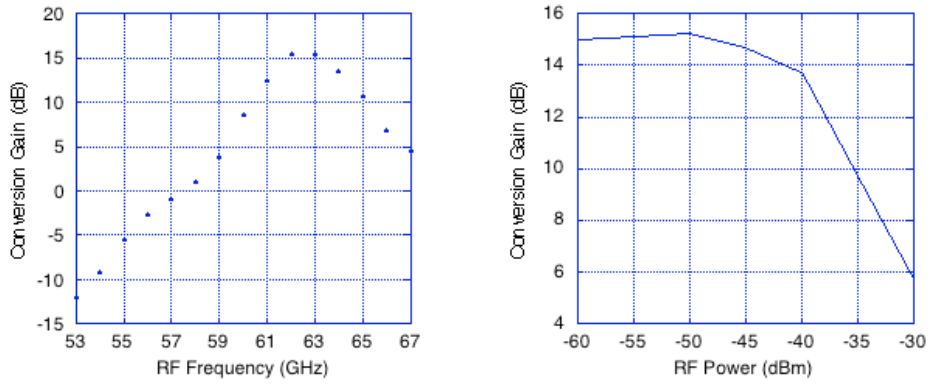


Figure 5.17. (a)Block diagram and (b) die photograph of the subharmonic 60 GHz receiver front-end.

The front-end can also be fine tuned for a direct down-conversion architecture. The front-end is fabricated with the integrated cross-coupled voltage-controlled oscillator with a cascode amplifier as described in 5.4.1.1. The co-design issues are similar to that described in 5.4.2.

Measurements have been performed in the integrated receiver front-end chips to determine the conversion gain, bandwidth, and linearity of the LO power. The integrated LNA-mixer-VCO module consumes a total of 62 mW (27 mW from LNA, 0 mW from mixer, 20 mW from VCO, and 15 mW from VCO-amplifier). A 15.5 dB conversion gain is achieved for the integrated receiver front-end with the on-chip cross-coupled oscillator. Figure 5.18a shows the measured conversion gain vs. RF frequency, and Figure 5.18b shows the measured conversion gain vs. RF power for the integrated LNA-mixer-VCO.



(a) **(b)**

Figure 5.18. (a) Conversion gain of the LNA-mixer-VCO vs. RF frequency (VCO tuned to 30.4 GHz, 62 GHz RF); (b) Conversion gain of the LNA-mixer-VCO vs. RF power (VCO tuned to 30.4 GHz, 62 GHz RF).

The 3-dB RF bandwidth is around 4 GHz. The measurement results indicate a –40 dBm of input 1-dB compression point. The measured noise figure of a separate front-end amplifier test structure is approximately 8 dB. Hence, the estimated noise figure of the receiver chain is less than 10 dB.

The measurement results indicate an excellent performance of the 60 GHz sub-harmonic front-end in low-cost 0.18 μm SiGe. The conversion gain of around 16 dB can be attributed to the high gain of the front-end LNA (~ 25 dB), and low conversion loss of the passive sub-harmonic mixer (~ 9 dB). The on-chip VCO output power (after the amplifier) can be estimated at around 4.5 dBm from the characteristics of the LNA-mixer with the external LO. This is the first report of a 60 GHz receiver front-end in 0.18 μm SiGe with the comparable performance to high-end IC processes. The front-end is extremely low power and can be tuned to heterodyne or direct-conversion architectures with minimal changes.

5.4.4 Design and layout of integrated VCO-PLL for MMW systems

In section 4.2, the integrated VCO-PLL or the frequency synthesizer block is identified as the most parasitic sensitive block in a MMW transceiver implementation. In

chapter 4, the effects of parasitics in different frequency dividers and VCOs in 90 nm CMOS process are demonstrated. In this sub-section, the significance and optimization of parasitics in separate blocks of an integrated frequency synthesizer are demonstrated. Also, the layout complexities are explained for a specific implementation of the VCO-PLL. The frequency synthesizer block diagram is shown in Figure 5.19. The center frequency of the VCO is chosen as 53 GHz, considering the RF frequency as 61 GHz and IF frequency as 8 GHz. The 53 GHz to 26.5 GHz frequency division is achieved using an injection-locked divider (ILD). The VCO differential outputs are connected to the differential amplifier and injection-locked-divider. The amplifier outputs are fed to the mixers. The ILD outputs are applied to the divide-by-512 block considering a 52 MHz crystal reference frequency. Other programmable dividers can be used for multi-channel applications for a different frequency planning.

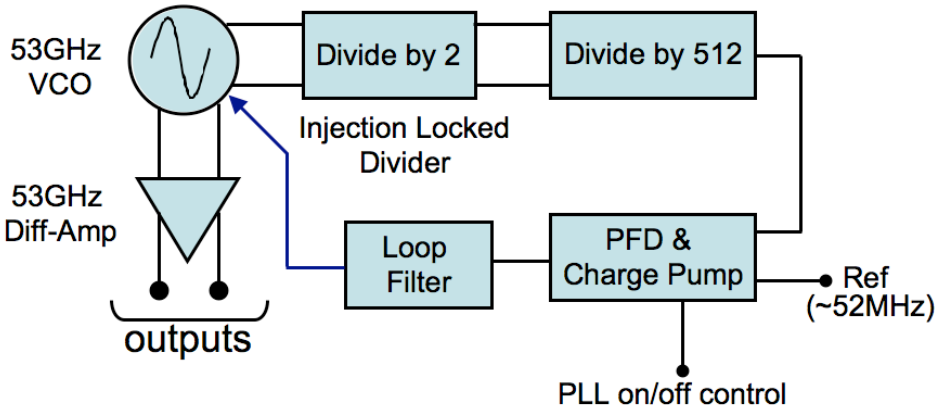


Figure 5.19. The frequency synthesizer block diagram.

VCO & Injection locked divider (ILD):

A cross-coupled oscillator is used to generate 53 GHz signal. The schematic with injection locked divider is shown in Figure 5.20. The injection locked divider is designed using a cross-coupled configuration with free running frequency of 26.5 GHz. The 53 GHz differential signals are injected on the oscillating nodes as shown in Figure 5.20.

Both NMOS and PMOS injections are used. For the layout constraints of cross-coupled cores and the tuning micros-trip lines, the feeding lines to ILD have parasitic components that transfer the input impedances of injection devices to different levels from just capacitive components. Thus, for the design of differential amplifier, these parasitic networks are evaluated accurately. The VCO and ILD both are implemented using the parasitic benchmarking procedure described in section 3.4.

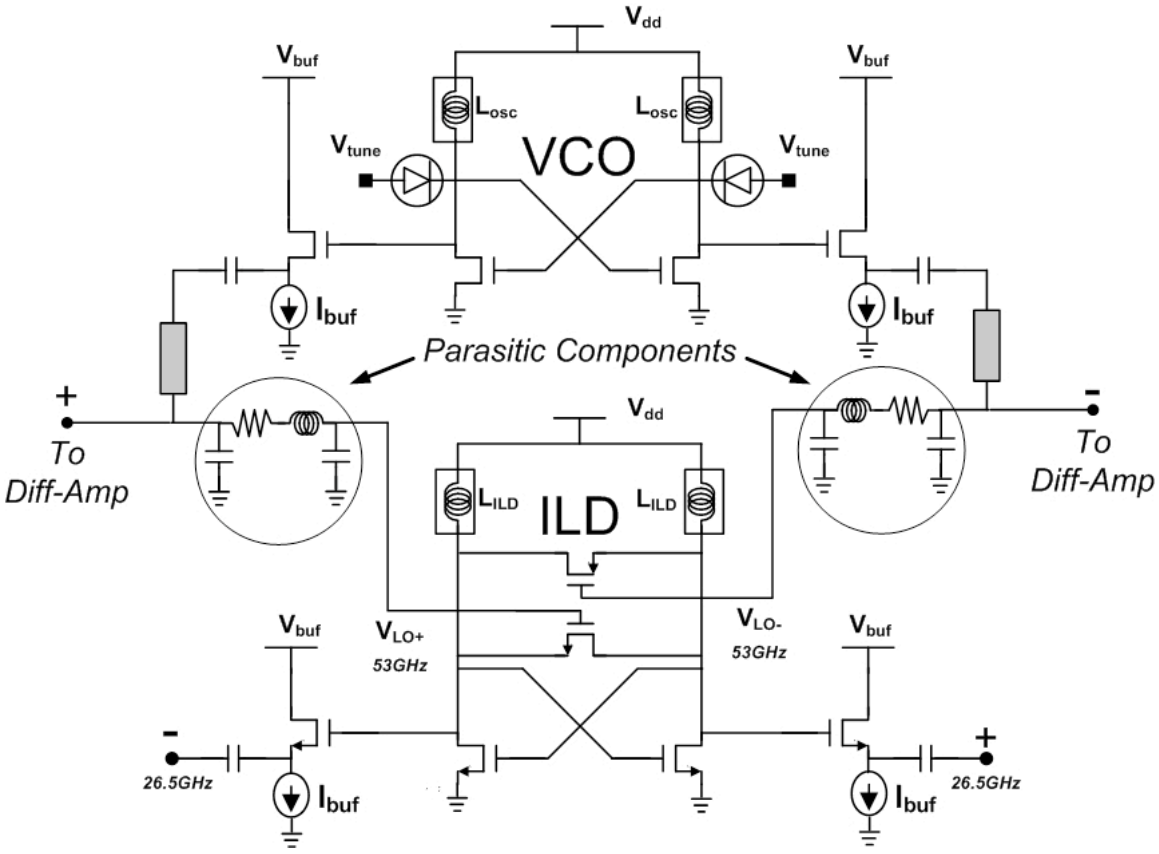


Figure 5.20. The schematic of integrated VCO with injection-locked-divider.

Differential amplifier:

The source-follower buffer outputs of the VCO are fed to a differential amplifier. The input matching is simplified as an inductive line. The output matching networks are designed according to the matching requirements for RX and TX mixer driven by the

layout constraints. The schematic of the differential amplifier is shown in Figure 5.21. The power consumptions are 9 mW and 15 mW to provide LO power of -2 and +3 dBm for receiver and transmitter respectively.

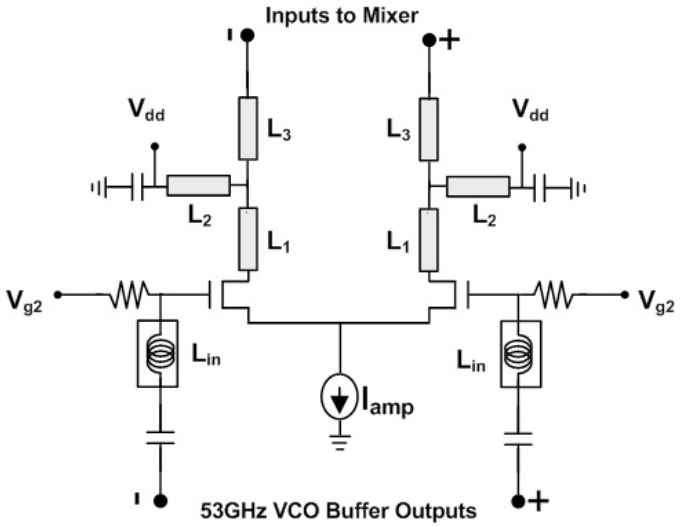


Figure 5.21. The schematic of differential amplifier.

Divide-by-512 block:

The divider block diagram is shown in Figure 5.22. The divider includes nine stage dividers (i.e. divide by 512). The first three stages use a D-type master-slave flipflop-based dividers. The last six stages use conventional D-flipflop based dividers. It exhibits a power consumption of 10 mW. For a >200 mV amplitude input signal, this divider can divide frequencies ranging from 18 GHz to 32 GHz. The dividers are designed considering the parasitic effects as described in subsection 4.4.3. The parasitics at the sensitive nodes are minimized to have the maximum swing at the divider output with given DC power consumption.

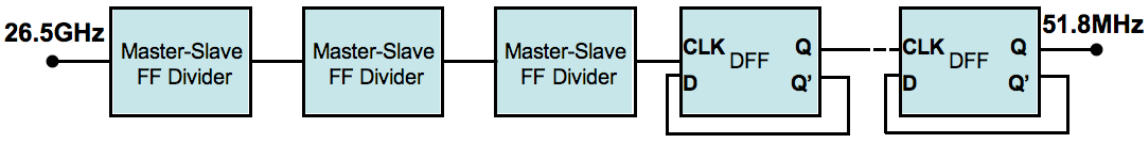
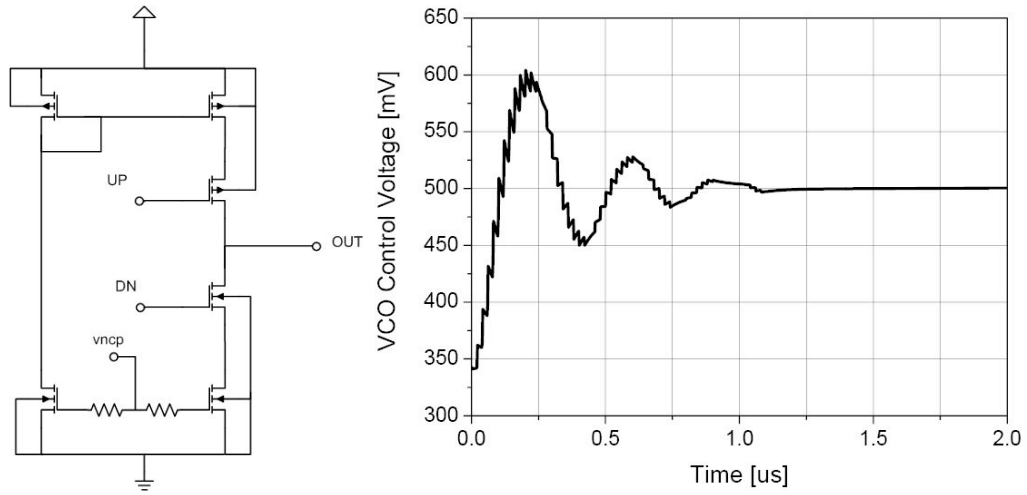


Figure 5.22. Divide-by-512 block diagram.

Phase frequency divider (PFD), charge pump and loop filter:

The PFD has been implemented using the combinatorial single-edge type architecture. The charge pump implements a conventional single-ended topology with enclosed biasing circuitry to the extent of controlling the output current by means of a single voltage input (vncp) as shown in Figure 5.23a. This voltage can be used as the PLL on/off (PLLC) controls. The loop filter is a passive RC type. Figure 5.23b shows the VCO control voltage for a frequency step of 1 MHz of the reference frequency from 52 MHz to 53 MHz. The locking time is shown to be roughly equal to 1.1 μs. Since these circuits work at MHz frequencies, the effects of parasitics are less but still the ground resistances have to be reduced. Also, the loading at different paths for very long connections in an integrated chip is considered.



(a) **(b)**

Figure 5.23. (a) Charge-pump schematic, (b) PLL control voltage for 1MHz reference frequency step.

Now, the main parasitic sensitive portions of this VCO-PLL implementation are shown in Figure 5.24. In the complete layout, these portions are identified as:

(i) The cross-coupled core for the 53 GHz VCO

(ii) The feeding of 53 GHz cross-coupled outputs to the ILD.

(iii) The cross-coupled core of 53 GHz ILD.

(iv) The feeding of 26.5 GHz outputs to the divider chain.

(v) The first three stages of dividers in the divider chain.

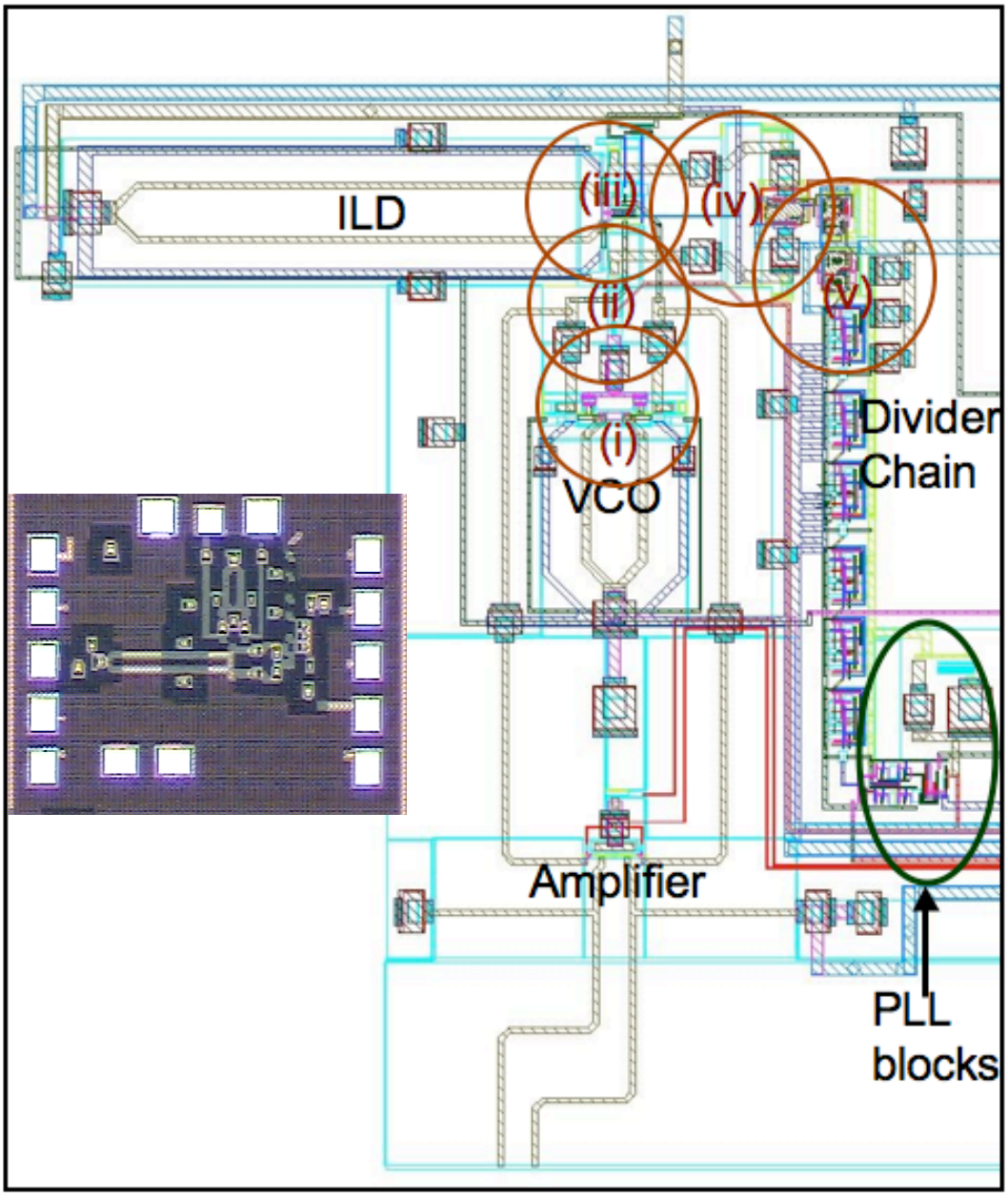


Figure 5.24. The layout and die photo of the integrated VCO-PLL.

The cross-coupled core for VCO and ILDs are analyzed as described in section 3.4 and 5.2. The input feeding lines for ILD are represented as interconnect RLC networks.

The 26.5 GHz ILD outputs are mostly routed through 50-ohm transmission lines and just before applying to the first stage of divider chain, the power is converted to voltages using on-chip resistances. The parasitics in first three stages of dividers are considered as demonstrated in section 4.4.3. The considerations of parasitics for different blocks and the proposed solutions are summarized in Table 5.3. The most challenging task is to operate all these parasitic sensitive blocks in their desired frequency ranges for a working frequency synthesizer.

Table 5.3. Parasitic considerations for integrated frequency synthesizer

Layout blocks	**Considerations => Solutions**
Cross-coupled VCO [portion (i)]	Parasitics can cause up to 30% shifts => Parasitic benchmarking (section 3.4) and design optimization including parasitics (section 5.2)
VCO to ILD feeding [portion (ii)]	Shifts of input impedances => Accurate parasitic estimation using EM-trained neural network models (section 3.3)
ILD cross-coupled core [portion (iii)]	Parasitics can cause up to 20% shifts => Parasitic benchmarking (section 3.4) and design optimization including parasitics (section 5.2)
ILD to divider chain feeding [portion (iv)]	Loading of dividers and output matching for ILD => Transmission line implementation and accurate parasitic estimation using EM-trained neural network models (3.3)
Master-slave FF-based dividers [portion (v)]	Shifts of frequency division ranges => Accurate parasitic estimation using EM-trained neural network models (section 3.3) and design optimization using sensitive node analyses (section 5.2)
DFF-based dividers	Degrading effects of parasitics on the maximum operating frequency => Accurate parasitic estimation using EM-trained neural network models (section 3.3)

5.4.5 Examples of parasitic sensitivity in MMW systems

In this sub-section, the 57-64 GHz license-free band is considered to understand the sensitivity towards parasitics for different modulation schemes. For MMW applications, the modulation scheme has to be chosen considering the trade-off between the bit rate and complexity of the hardware. The simplest coherent modulation scheme is BPSK that can provide a bit rate of 3.5 Gbps (upto 5 Gbps with baseband filtering), if the entire 7-GHz-bandwidth is utilized. QPSK can double the bit rate, but QPSK requires quadrature mixers and higher sensitivity of the receiver front-end. QAM can double the bit rate as compared to QPSK, but QAM requires a stringent linear operation of the front-end. Amplitude modulation has been explored up to 1.5 Gbps data rate for video applications [2.9]. ASK is the simplest architecture, but it is limited by the capacity and SNR. Frequency-shift keying (FSK) and Gaussian-minimum-shift keying (GMSK) are other relatively simple modulation schemes that can be utilized in a 60 GHz system. Minimum-shift-keying can be realized from an FSK system with the frequency difference between on and off states being half of the bit rate.

Among all these modulation schemes, integrated PLL is used for all coherent schemes and even for non-coherent schemes like ASK to get an accurate LO frequency. For FSK or MSK modulations, the frequency variations are obtained from the VCO by applying the base band data to the VCO control node. As identified earlier, VCOs and frequency dividers are the most parasitic-sensitive blocks in the system implementation. While working, VCO-PLL integration gives a fixed frequency output to the mixers. The frequency should not change though the control voltage in locked state may vary from chip to chip with parasitic and process variations. The phase noise of locked-VCO and

the output power fed to the mixer are important system performance parameters. Among other blocks, amplifiers and mixers are mostly transmission-line-based designs. The co-design and co-optimization challenges are already described in sub-sections 5.4.1 through 5.4.4. Also, it is assumed that the integrated layout issues as described in section 5.3 are taken cared of the integrated system layout.

In this sub-section, frequency-shift-keying scheme is studied to understand the effect of parasitics in a system performance. For implementation, a cross-coupled VCO (section 4.4.2) centered around 60 GHz in CMOS process is considered. The schematic representation of the FSK/MSK system in a module implementation is shown in Figure 5.25. The off-chip 50-ohm transmission line used to feed data is T1. Since the source is in 50-ohm environment, the line T1 will give a small loss at sub-5GHz frequencies. L1 and C1 represent the bond wire inductance and the pad capacitance respectively. T2 represents an on-chip transmission line to reach the VCO block from the pad. After the transmission line, the on-chip parasitics are shown as L2, R2, and C2.

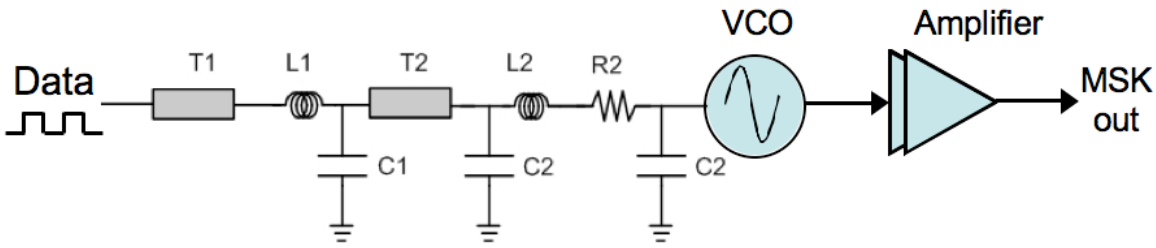


Figure 5.25. The FSK/MSK system with the data-feeding network.

The effects of bond wire inductance on the FSK frequency output with an input of 1 GHz square wave is shown in Figure 5.26a. The same effect is observed in a 2 Gbps random data bit sequence. The inductive effects are observed as the ripples in the instantaneous frequency. Also, the parasitics in the cross-coupled nodes are critical for the VCO gain and hence, the frequency difference in on and off states. For the same

center frequency, the percentage variations of frequency for a given data rate (2 Gbps in this case) with different values of extra parasitic capacitances to the cross-coupled oscillator nodes are shown in Figure 5.26b.

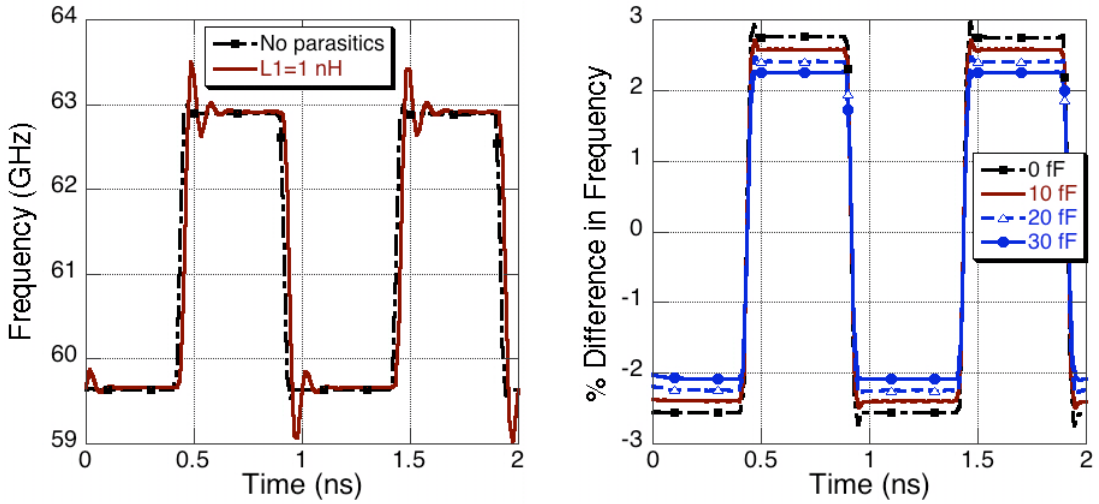


Figure 5.26. The variation of frequency with data for (a) different bond wire inductances and (b) different parasitic capacitance at oscillation nodes.

The input on- and off-state voltages are fixed to 100 mV and 900 mV respectively. The decreasing trend of percentage difference of frequencies signifies the decrease of VCO gain (K_{VCO}). That is explained from the reducing value of $\frac{(C_{\text{var max}} + C_{fixed})}{(C_{\text{var min}} + C_{fixed})}$ where varactor capacitances ($C_{var\ max}$ and $C_{var\ min}$) are not changing but C_{fixed} is increasing.

Similar effects are observed in an MSK modulation scheme. For more advanced system implementation like phased-array systems, the compactness of layout will demand aggressive shrinking of each blocks, and in such scenarios, the ground continuity, power supply resistances and interconnect parasitics are critical parameters for layout and performance optimizations.

5.5 Summary

In this chapter, the co-design and co-optimization tasks are described with a stress on the role of parasitics. A cross-coupled VCO is chosen to demonstrate a systematic design and yield optimization technique including the parasitics. Artificial intelligence approaches are used to make the design and yield optimization fast, automated, and systematic. Thereafter, the importance of layout optimization for a complete system is described with layout guidelines to reduce the failure and performance degradation possibilities due to on-chip and off-chip parasitics. Then the co-design approaches are demonstrated using system blocks, e.g., VCO-amplifiers, frequency synthesizers including PLL, and integrated LNA-VCO-mixer. Measurement results are reported for some of the co-design examples implemented in CMOS and SiGe-BiCMOS processes. Later, parasitic sensitivity of an MMW-system example is shown for a frequency-shift-keying approach.

Chapter 6

Conclusions and Future Work

6.1 Technical contributions

In this dissertation, the importance of estimation and optimization of layout parasitics in MMW circuit design flow is investigated. Different circuit design- and layout-examples are considered with stress on the inclusion and optimization of wire/interconnect parasitics. A novel methodology is proposed to reduce the number of design-passes and to optimize including parasitics effectively. Measurement results of several circuits that are implemented in state-of-the-art CMOS and SiGe-BiCMOS processes are used to support the role of parasitics and the design methodology including parasitics.

In the second chapter, the available methods for characterizing the parasitic effects are described. A broadband interconnect model is studied, and the criticality of substrate network is described. The sensitivity of design performance parameters and hence, the importance of extraction accuracy and standardization of extraction methodologies are demonstrated.

In the third chapter, a novel automated verification procedure [3.2] for parasitic extraction methodologies is described. Matlab codes with perl scripts are used to generate test layouts, and accordingly, these structures are used to compare the existing parasitic

extraction tools with a 3-D EM tool or the " gold standard" [3.8]. Layouts of ring oscillators as examples of functional active circuits are generated using the same procedure, and these layouts are incorporated as parasitic-benchmarking test structures in a 90 nm CMOS process (provided by IBM Corporations). The measurement results of these ring oscillators are used for the final verification of parasitic extraction (PEX) tools [3.2]. This automated extraction method is not only limited to verification of PEX tools, but this methodology can also be used for building test-sites and modeling active as well as passive structures in different technologies.

Neural-network-based models are used to demonstrate the effectiveness of artificial intelligence techniques for characterizing parasitic components [3.8]. The models are trained using EM tools. To make it compatible with the automated generation methodology, Matlab platform is used to model wire resistances, capacitances and inductances for a multi-layer process. Measurement results of meander lines are used to show the effectiveness compact test structures.

A parasitic benchmarking procedure at millimeter-wave frequencies is demonstrated using cross-coupled oscillators for a 90 nm CMOS process (provided by ST Microelectronics). Five oscillators with frequencies varying in the range of 44 to 55 GHz are implemented and measured for different DC bias conditions to model the layout parasitics and the transmission-line effects. Some of these oscillators for specific conditions are used to model the parasitics, and the rest of the data points are used to verify the proposed methodology. This benchmarking procedure is not limited to this frequency range. Varying the tuning inductance lengths, this methodology can also be used at even higher frequencies for defense applications. Oscillators are selected to

choose the oscillation frequencies as the test parameters. VCOs can also be used with center frequency and tuning ranges as test parameters for parasitic benchmarking.

In the fourth chapter, the complete transceiver architectures for different modulation schemes are studied to identify the circuit blocks that are more sensitive to interconnect parasitics. The parasitic effects on transistors for CMOS and SiGe-BiCMOS processes are illustrated. The critical components in transistor structures are described, and the parasitic effects on active device performances are demonstrated. The circuits are designed for the worldwide license-free 59-64 GHz band (59-66 GHz in Japan and Europe, 57-64 GHz in USA) [1.2], targeted for multi-gigabit transmissions.

Layouts are differentiated into two types depending on their parasitic sensitivities. Parasitic-sensitive circuits, e.g., fixed-frequency oscillators, VCOs, and frequency dividers, in millimeter-wave frequencies are designed and implemented in state-of-the-art processes to demonstrate the criticality of layout in MMW circuit design flow. Among fixed-frequency oscillators, a negative–resistance SiGe-HBT oscillator is implemented using a single transistor, and it has a measured phase noise close to -100 dBc/Hz at 1 MHz offset at 60 GHz. CMOS oscillators at 63-66 GHz using 130 nm NMOS devices are used to demonstrate the parasitic effects closer to the technology limits. Different cross-coupled and push-push VCOs are implemented with operating frequency ranging from 30 to 65 GHz. VCOs are implemented for both direct-conversion and super-heterodyne architectures for 60 GHz applications. Four test structures of frequency dividers are measured to show a large shift from the simulation set up without parasitic components. The effects due to transistor models and parasitics are demonstrated using these master-slave flipflop dividers [4.10]. Even though MMW amplifiers are designed based on

transmission line models and measurements from transistor test structures, still the degrading effects of on-chip and off-chip parasitics in sensitive nodes are shown for low-noise-amplifier and power-amplifier examples at 60 GHz.

Substrate effects cannot be neglected for the effects of parasitic capacitances between signal lines and substrate nodes. The effects of substrate resistance on interconnect capacitances are shown using measurement results from test structures. Using simulation results of MMW circuits, the substrate effects are demonstrated in different technologies.

In the fifth chapter, the co-design and co-optimization issues are deciphered using MMW system blocks. In a design-centering procedure [5.1, 5.2] using neural networks for modeling and genetic methods for optimization, cross-coupled VCOs at MMW frequencies are systematically optimized including layout parasitics. A parasitic sensitivity analysis is incorporated with a sensitive node analysis to figure out the dominant parasitic components as well as the most-affected design nodes.

The layout optimization guidelines for MMW circuits and system-implementations are discussed, and different examples are cited to stress on the role of parasitics. The co-design and co-optimization methods are demonstrated using different sections of a transceiver, e.g., VCO-amplifiers, up/down converters, and integrated VCO-PLL. A cross-coupled VCO is co-designed with a cascode amplifier in SiGe-BiCMOS process, and the same structure is integrated with mixer to act as an up/down converter with a measured RF bandwidth of 9 GHz. The integrated converter is used with LNA in a low-cost receiver application at 60 GHz. Also, a frequency synthesizer is implemented in 90 nm CMOS process, and the methodology to optimize/minimize the effects of parasitics in different blocks of this integrated VCO-PLL are described.

Thus, this dissertation covers the estimation, modeling, and optimization of parasitic effects as well as verification of extraction methodologies for RF/MMW applications. The parasitic sensitivities for selected millimeter-wave circuits are demonstrated, and a parasitic benchmarking procedure is developed. The design centering procedure including parasitics is described to support the proposed methodology for accurate estimation and optimization of layout parasitics in a MMW circuit/system design flow.

6.2 Future research directions

In this section, the future research directions are described. The scopes of different topics discussed in this dissertation are mentioned, and the application space for this work is discussed.

6.2.1 Parasitic extraction, modeling and accuracy of design platform

In this work, ring oscillations are used for verifying the resistance- and capacitance-extraction methodologies. Also, cross-coupled VCOs at MMW frequencies are used to benchmark RLC extractions. But a more extensive verification procedure can be developed based on the automated layout generation approach. Since, the layout-generation code is technology-independent, this methodology can be used for any technology to generate a large set of test structures very fast. Different layout scenarios can be incorporated in these test structures to train the neural networks or the parasitic extraction tools to be used. The meander line structures can be used to model the parasitic resistances and capacitances at DC or low frequencies. For higher frequency characterizations of capacitances, straight-line structures can be laid out inside the ring oscillators with lesser number of inverter stages. Also, separate structures can be modeled

using 1-port/2-port S-parameter measurement results. For characterizing the inductances, cross-coupled oscillators in different frequencies can be used as shown in Figure 6.1a. Automated layout generation can be used to create different oscillator structures changing the tuning inductance lengths. In addition, the parasitic capacitances can be modeled in an already characterized benchmarking setup changing the inductances and capacitances as shown in Figure 6.1b. The inductances can be varied as L_{OSC} or as a part of it. The coupling capacitance and to-ground or to-substrate can be represented as C1 and C2 respectively. From the VCO tuning characteristics, the parasitic RLC components can be back calculated at millimeter-wave frequencies.

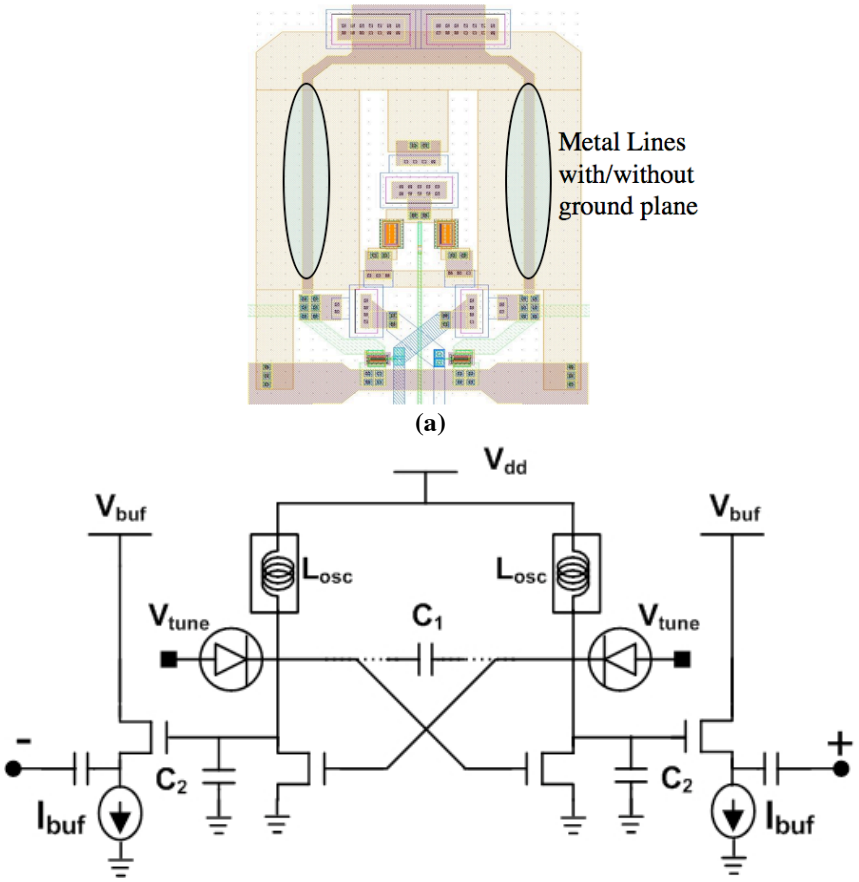


Figure 6.1. (a) Tuning inductance in the layout, (b) inductances and capacitances in a parasitic benchmarking set up.

6.2.2 MMW circuit design and layout optimization

A fully integrated silicon-based MMW transceiver at 60 GHz or higher frequencies has become the driving force for recent research activities in integrated MMW circuit designs. Even, in the digital domain, the frequencies are at gigahertz ranges, and hence, the layout optimization becomes critical in digital circuits as well. In an integrated transceiver, the layout optimization is not only important for RF blocks but they are also important in compact base-band solutions. The neural-network-based models for parasitic networks can be included into automated digital layout approach.

6.2.3 Design centering and genetic optimization in other MMW circuits

In this dissertation, design centering and systematic design optimization methodologies are shown for some VCO examples. The design centering is also important for other circuits. For example, in power amplifiers, the design of input/output/inter-stage matching networks is critical for the ranges of input and output impedances while using large devices to meet the power and efficiency requirements. The loss from matching networks demands an optimized impedance conversion to maximize the gain or P_{1dB} as required. A design centering procedure needs to be used to find matching networks insensitive to slight variations of transmission line characteristics for a given transistor size and DC conditions. The proposed methodology is summarized in Figure 6.2. Genetic optimization or gradient-method-based optimization methods can be used to reach an optimum point.

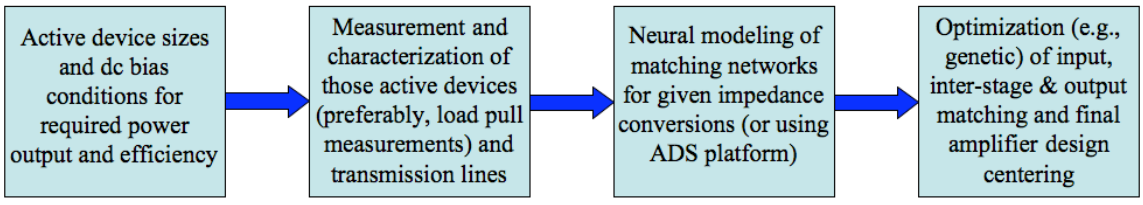


Figure 6.2. The optimization of power amplifiers.

Not only for VCOs or amplifiers, artificial intelligent techniques can be used for various circuits at any frequencies. Neural networks can be used to characterize the circuit behavior, and an advanced optimization procedure can center the designs. In this dissertation, the modeling of layout parasitics is demonstrated using Matlab platform, and these models can be embedded into design optimization procedure developed using artificial intelligence techniques in the same platform.

6.2.4 MMW system design including parasitics

MMW system performance cannot be optimized until all the systems blocks are design-centered including parasitic components. The effects of parasitics are not that prominent in sub-5GHz analog circuit domain. But with transistors operating in their limits, layout optimization is as important as having an efficient design topology. The design flow includes layouts not only in the final level of implementation but also in the intermediate levels, where the design is optimized based on layout constraints and parasitic sensitivity analyses. Since, minimization is not always possible, design and parasitic optimization have to be done using a systematic procedure as described in section 5.2 (for few circuit examples). The same methodology needs to be used in other blocks of the transceiver. For final implementation on a module, off-chip parasitics need to be accounted as well. The effectiveness of artificial intelligence techniques in design optimization can be utilized even in the co-design and co-optimization levels for integrated circuits.

6.2.5 Present and future application space

In this dissertation, mostly applications related to multi-gigabit wireless transmission in 57-64 GHz band are considered. But, the analysis and methodologies are not limited to only these applications. The automated layout generation and test-structure development tools are used in IBM Corporation in various processes for parasitic benchmarking of technologies. The neural-network-based modeling approach is valid for a very wide frequency range. The design and layout optimization procedure can be applied to silicon-based transceiver design for automotive, radar and wireless-personal-area-networking (WPAN) applications. Some of the application spaces are pictorially represented in Figure 6.3.

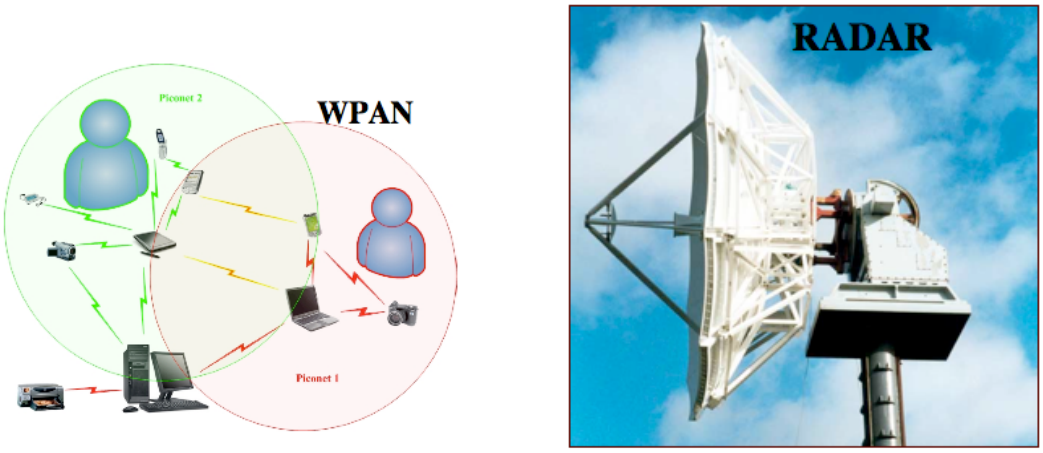


Figure 6.3. Applications in millimeter-wave.

The next wireless wave is going to be millimeter wave [6.1] and no integrated compact high performance millimeter wave system can be designed without accurate estimation and optimization of layout parasitics.

Appendix

Definitions of certain terms used in 2nd Chapter

Aggressor nets: The switching nets that induce noise on victim nets.

Differential pairs: One or more complementary pair of nets that provide noise immunity used for isolating paths without return paths.

Foster pair: A circuit composed of one resistor in parallel with one inductor used for modeling frequency dependent behavior of RL interconnects.

Forward coupling: In mutual inductance, a magnetic interaction between two different wire segments belonging to the same wire path.

Loop resistance: A sum of resistances of a signal line and its current return path.

Loop self-inductance: Inductance associated with a signal and its current return path.

Model order reduction: A way to reduce the number of elements in the parasitic netlist.

Mutual inductance: An electrical property of circuits that enables a current flowing in one conductor (or coil) to induce a current in a nearby conductor (or coil).

Mutual resistance: Any nonzero real parts of the off-diagonal elements in the loop impedance matrix.

Path: A unique two-point terminal connection (belonging to a wire net) between two devices.

Profile: An ordered list of adjacent layers and a loop resistance corresponding to a cross section of a wafer and describing the layer configurations for geometric generation.

Self-inductance: A property of a circuit whereby a change in current causes a change in voltage.

Skin depth: The distance from the surface of a conductor to where the current density has fallen to 1/e of its value at the surface.

Skin effect: A phenomenon occurring at high frequencies in which the current in a conductor's cross section tends to crowd on its surface.

Skin factor: A floating-point number that is multiplied by the skin depth to determine the nets to consider for skin effect modeling.

Victim nets: Nets on which noise is generated.

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Journal Publications:

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Invention Disclosures

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Vita

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